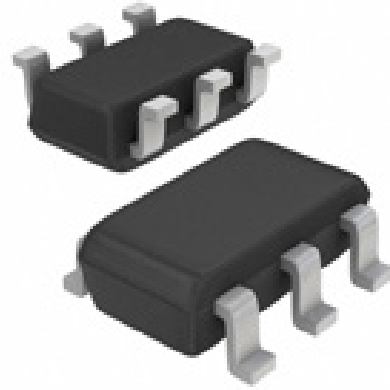


Features

- 1800Watts peak pulse power ($t_p = 8/20\mu s$)
- SOT23-6 package
- Solid-state silicon-avalanche technology
- Low clamping voltage
- Low leakage current
- Low capacitance ($C_j = 1.2pF$ typ.)
- Protection one data/power line to:
- IEC 61000-4-2 $\pm 30kV$ contact $\pm 30kV$ air
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 55A (8/20 μs)



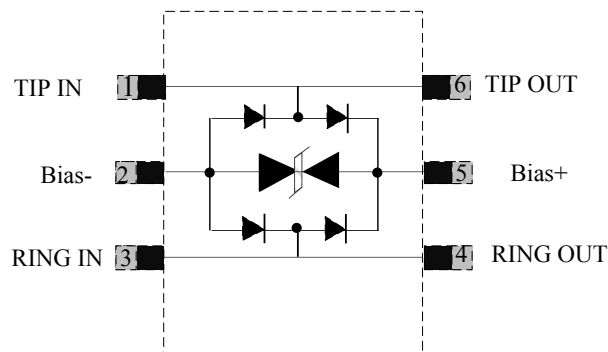
Applications

- ADSL, ADSL2+
- VDSL2, VDSL2+
- G.fast

Mechanical Data

- SOT23-6 package
- Molding compound flammability rating: UL 94V-0
- Packaging: Tape and Reel
- RoHS/WEEE Compliant

Schematic & PIN Configuration



Absolute Maximum Rating

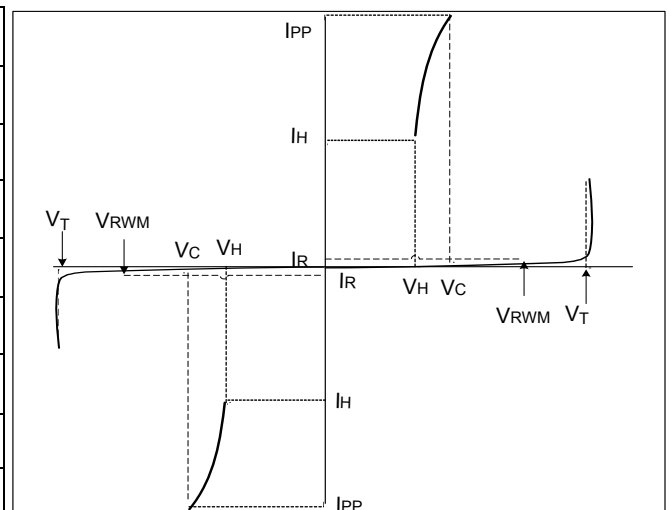
Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PP}	1800	Watts
Peak Pulse Current ($t_p = 8/20\mu s$) (note1)	I_{PP}	55	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	30 30	kV
Lead Soldering Temperature	T_L	260(10seconds)	°C
Junction Temperature	T_J	-55 to + 125	°C
Storage Temperature	T_{stg}	-55 to + 125	°C

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{RWM}				8.0	V
Holding Voltage	V_H	$I_T = I_H$		3.0		V
Holding Current	I_H		50			mA
Reverse Leakage Current	I_R	$V_{RWM} = 8V, T = 25^\circ C$			500	nA
Clamping Voltage	V_C	$I_{PP} = 55A, t_p = 8/20\mu s$		35		V
Trigger Voltage	V_T			13	15	V
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$ Line to Line		1.2		pF

Electrical Parameters (TA = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current



Note.: 8/20μs pulse waveform.



Typical Characteristic Curves

Fig.1 Peak Pulse Power Rating Curve

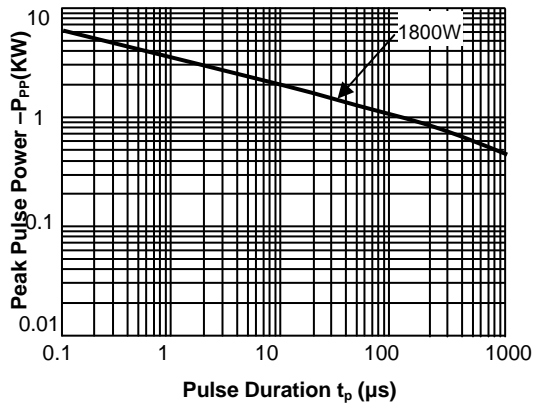


Fig.2 Pulse Derating Curve

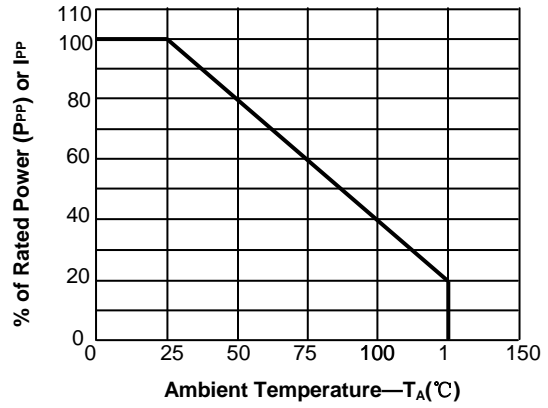


Fig.3 Pulse Waveform-8/20μs

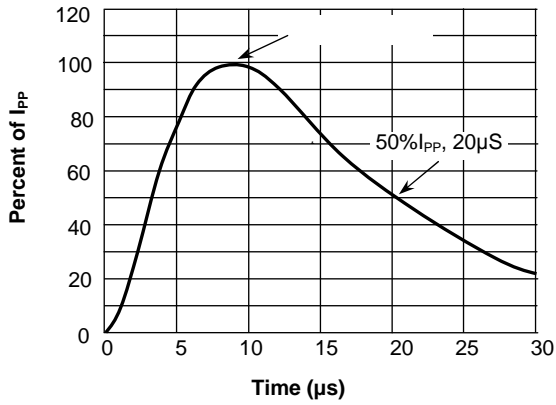
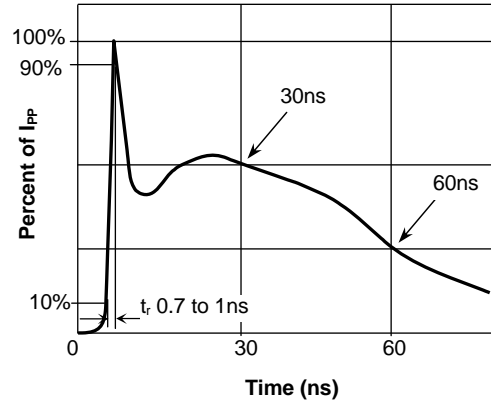


Fig.4 Pulse Waveform-ESD(IEC61000-4-2)



Application

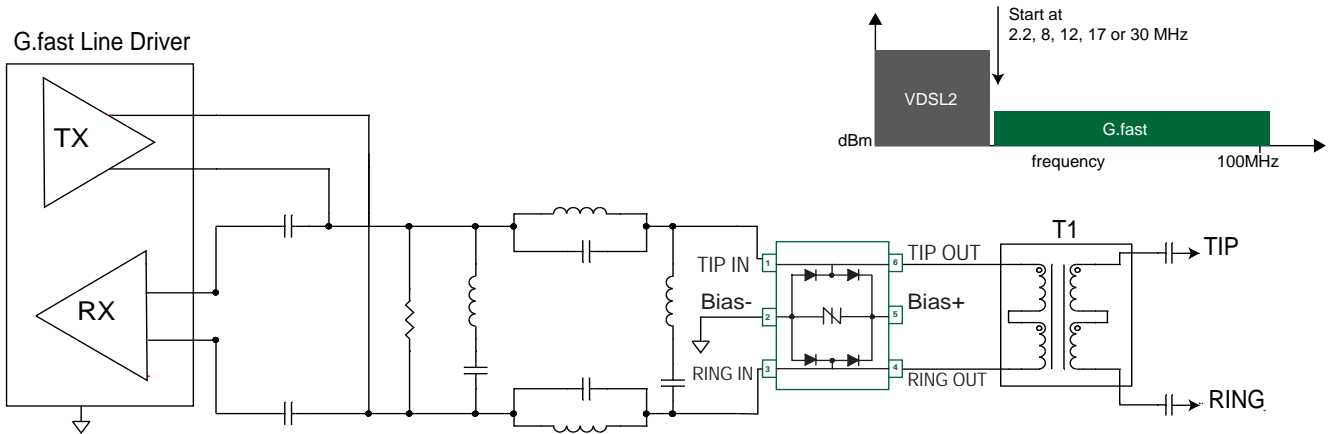
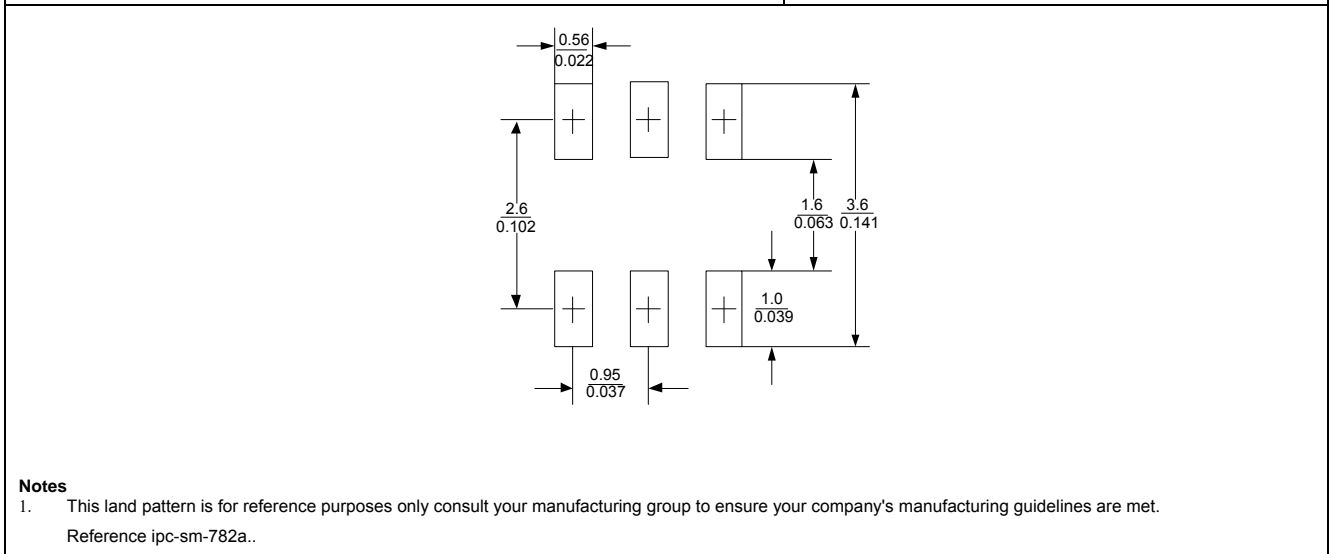
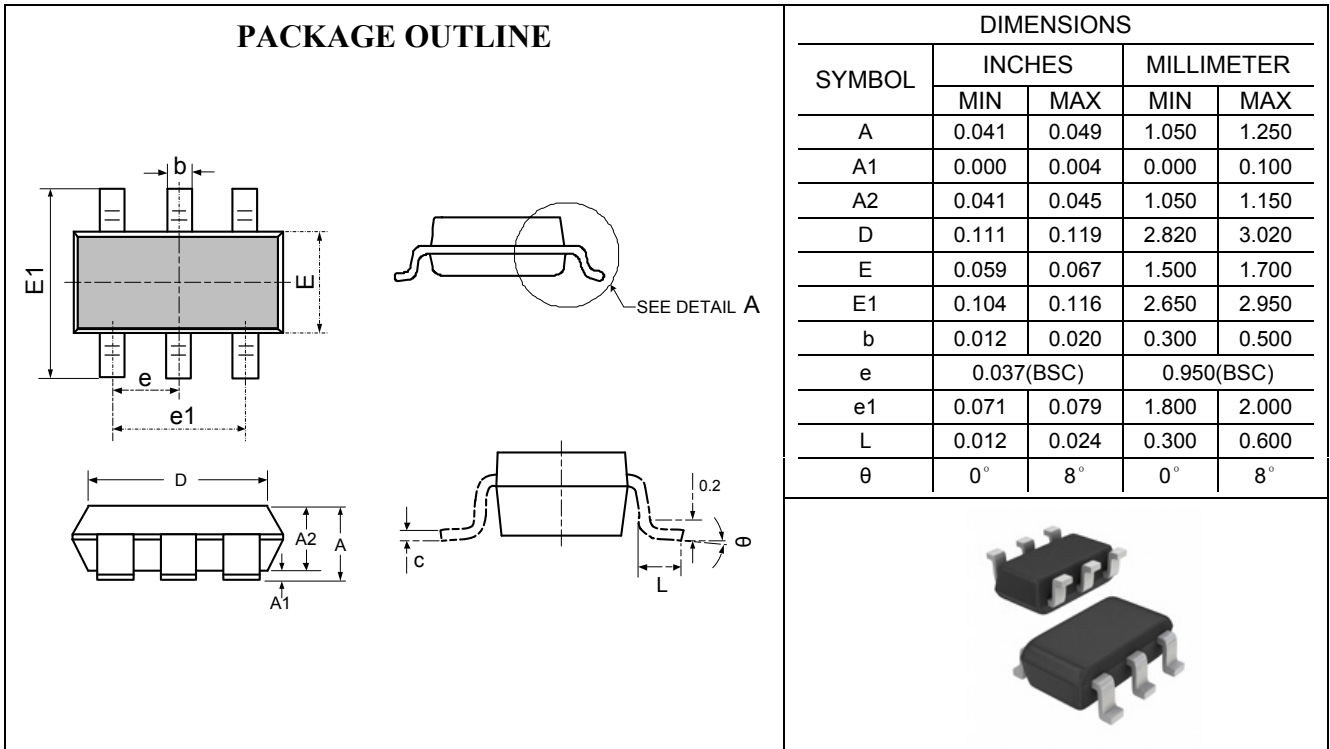
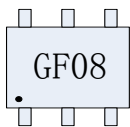


Fig.5 G.fast protection

The “Bias -” lead can be connected to the line driver ground with the “Bias + ” lead left open so this solution provides both differential and common mode protection. Both “Bias -” and “Bias +” leads can be left floating for differential only protection and finally for capacitance variance sensitive applications, the “Bias -” and “Bias +” leads may have the appropriate polarity voltage (< VDRM) applied to further minimize any negative capacitance effects.



Outline Drawing – SOT23-6

Marking

Ordering information

Order code	Package	Base qty	Delivery mode
RLST236A082LCH	SOT23-6	3k	Tape and reel

