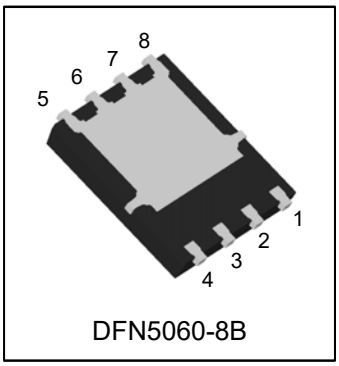
NA7616HD

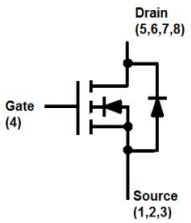
N-Channel Enhancement Mode MOSFET



DFN5060-8B

1. FEATURES

- Advanced trench cell design.
- Low Thermal Resistance.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



2. APPLICATIONS

- Motor drivers
- DC-DC Converter

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
NA7616HD	LN7616H	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain-to-Source Voltage	VDS	100	V
Gate-to-Source Voltage	VGS	±20	V
Continuous Drain Current(TC = 25 ℃, VGS =10 V)	ID	59	A
Pulsed Drain Current(TC = 25 ℃, VGS = 10 V)	IDM	236	A
Avalanche Current (L = 0.3mH)	IAS	23	A
Avalanche Energy (L = 0.3mH)	EAS	80	mJ
Power Dissipation(TC = 25 ℃)	PD	35	W
Operating Junction and Storage Temperature Range	Tj/Tstg	-55~+150	℃

5. THERMAL CHARACTERISTICS

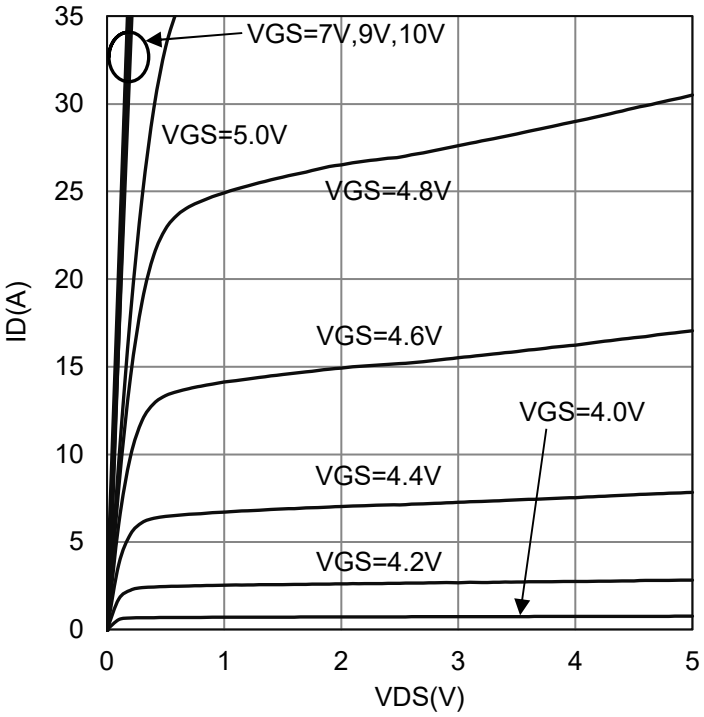
Parameter	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient(Note 1)	RθJA	62.5	℃/W
Thermal Resistance Junction-to-Case(Note 2)	RθJA	103	
Thermal Resistance Junction-to-Case	RθJC	3.5	

1. Surface Mounted on 1 in^2 pad area, t ≤ 10 sec
2. Surface−mounted on FR4 board using the minimum recommended pad size.

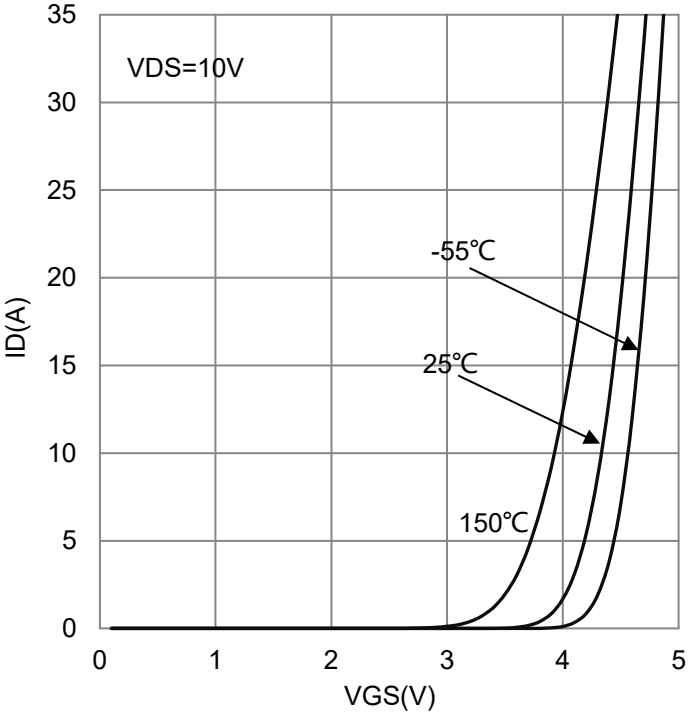
6. ELECTRICAL CHARACTERISTICS (Ta= 25ºC)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain to Source Breakdown Voltage (VGS =0V, ID =250μA)		BVDSS	100	-	-	V
Zero Gate Voltage Source Current (VDS =80V, VGS =0V)		IDSS	-	-	1	uA
Gate-Body current (VDS =0V, VGS = ±20V)		IGSS	-	-	±100	nA
Gate Threshold Voltage (VDS = VGS , ID = 250μA)		VGS(TH)	2	3	4	V
Drain-to-Source On-Resistance (VGS = 10 V, ID = 20 A) (VGS = 6 V, ID = 10 A)		RDS(ON)	- -	4.3 7	5.3 11	mΩ
Diode Forward Voltage (ISD = 20 A, VGS = 0 V)		VSD	-	0.82	1.2	V
DYNAMIC						
Input Capacitance	(VGS = 0V ,VDS = 50V, f = 1MHz)	Ciss	-	3353	-	pF
Output Capacitance		Coss	-	514	-	
Reverse Transfer Capacitance		Crss	-	10.3	-	
Turn-on Delay Time	(VDS=80 V, VGEN=10V,RG = 3.3 Ω,RL=4 Ω, IDS = 20 A)	td(ON)	-	24	-	nS
Rise Time		tr	-	29	-	
Turn-Off Delay Time		td(OFF)	-	56	-	
Fall Time		tf	-	24	-	
Total Gate Charge (VDD=50V,VGS=10V,ID=13A)		Qg	-	66.7	-	nC
Total Gate Charge (VDD=50V,VGS=5V,ID=13A)		Qg	-	38.4	-	
Gate to Source Charge (VDD=40V,VGS=5V,ID=68A)		Qgs	-	19.8	-	
Gate to Drain Charge (VDD=40V,VGS=5V,ID=68A)		Qgd	-	18.36	-	
Gate Resistance (VDS=0V,VGS=0V,f=1.0MHz)		Rg	-	0.95	-	Ω

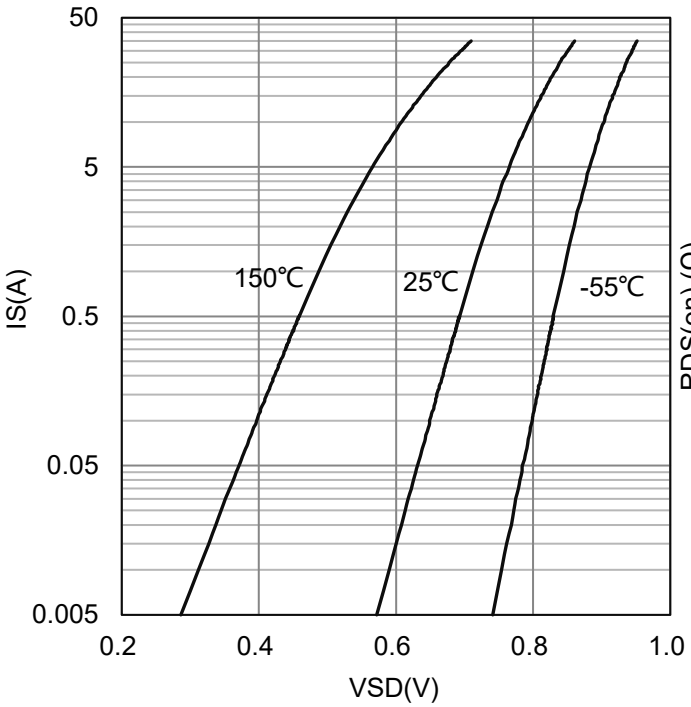
7.ELECTRICAL CHARACTERISTICS CURVES



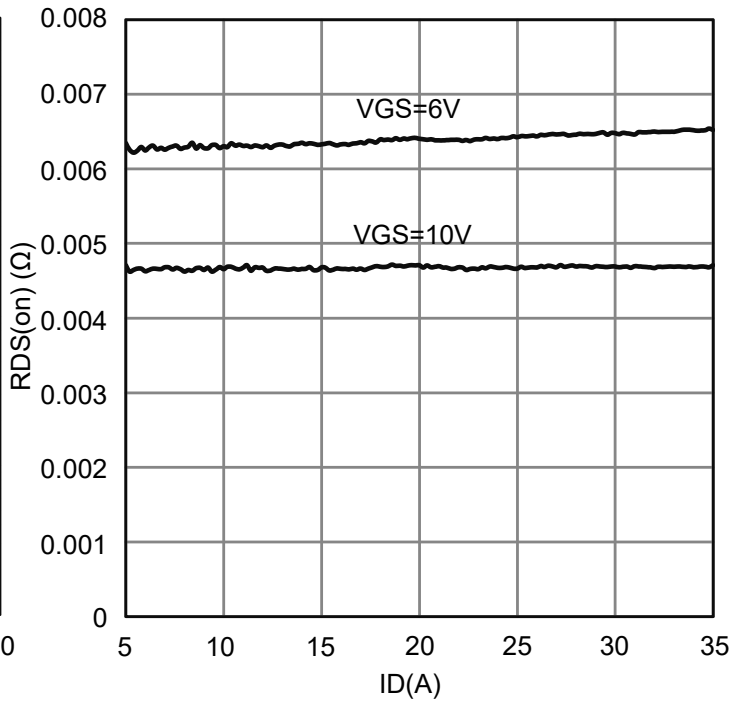
ID vs. VDS



ID vs. VGS

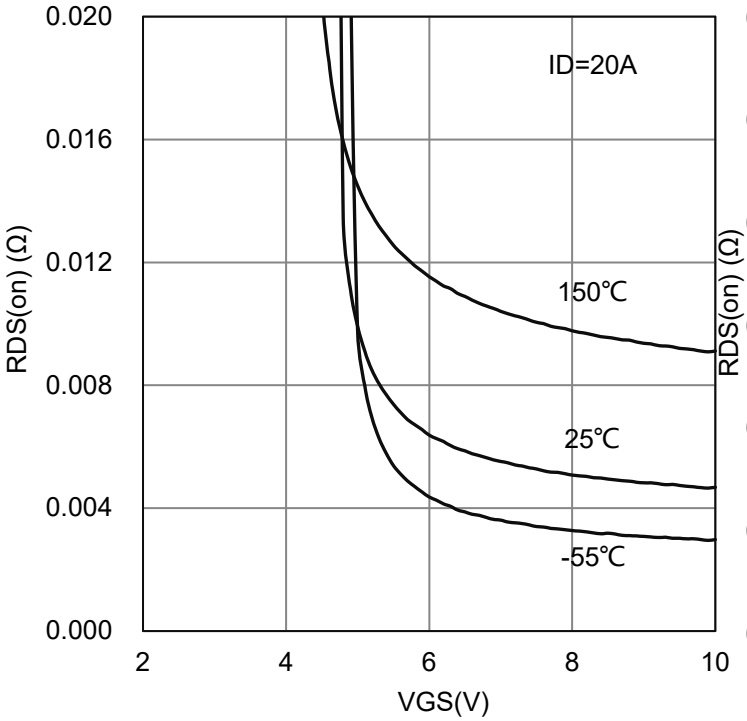


IS vs. VSD

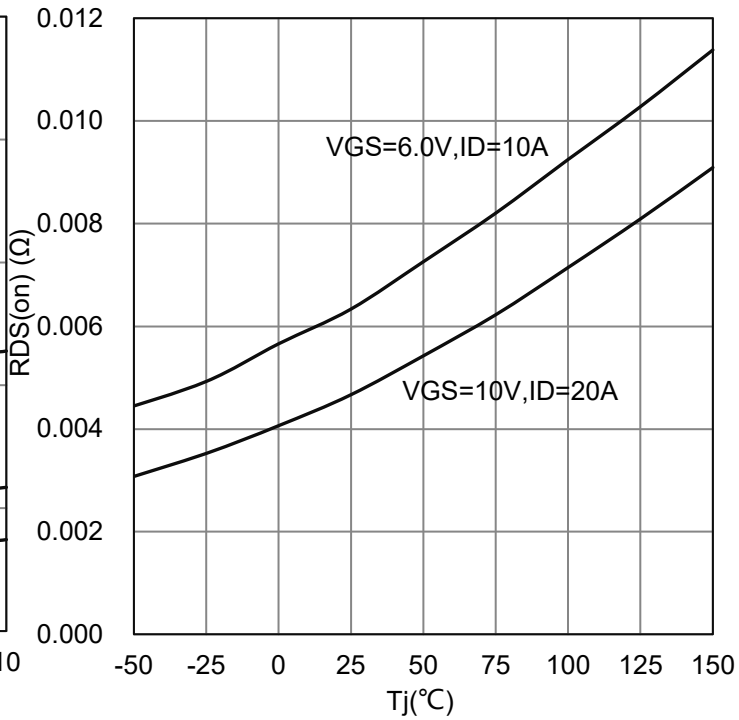


RDS(on) vs. ID

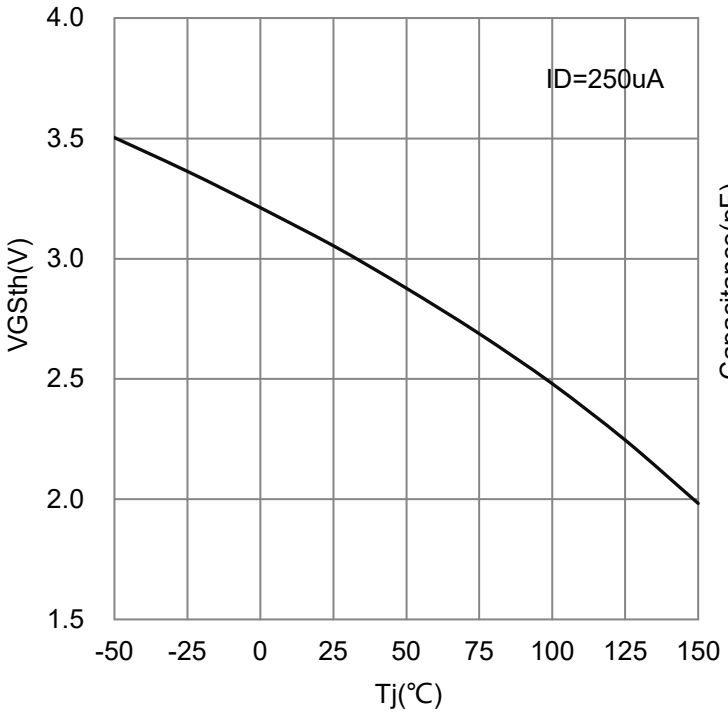
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



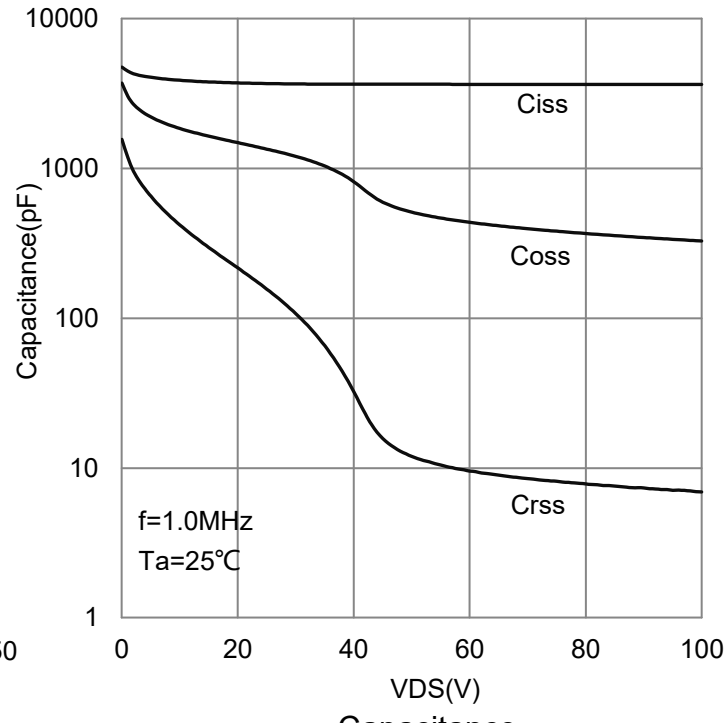
RDS(on) vs. VGS



RDS(on) vs. Tj

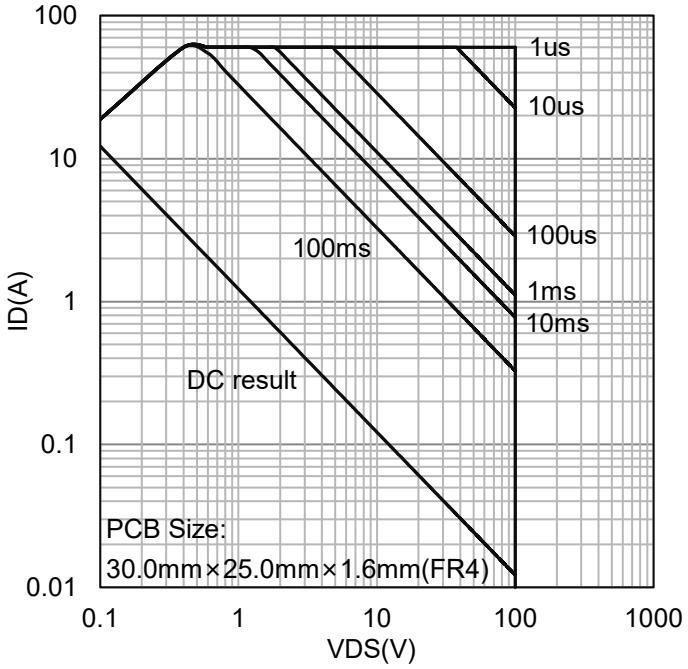


VGSth vs. Tj

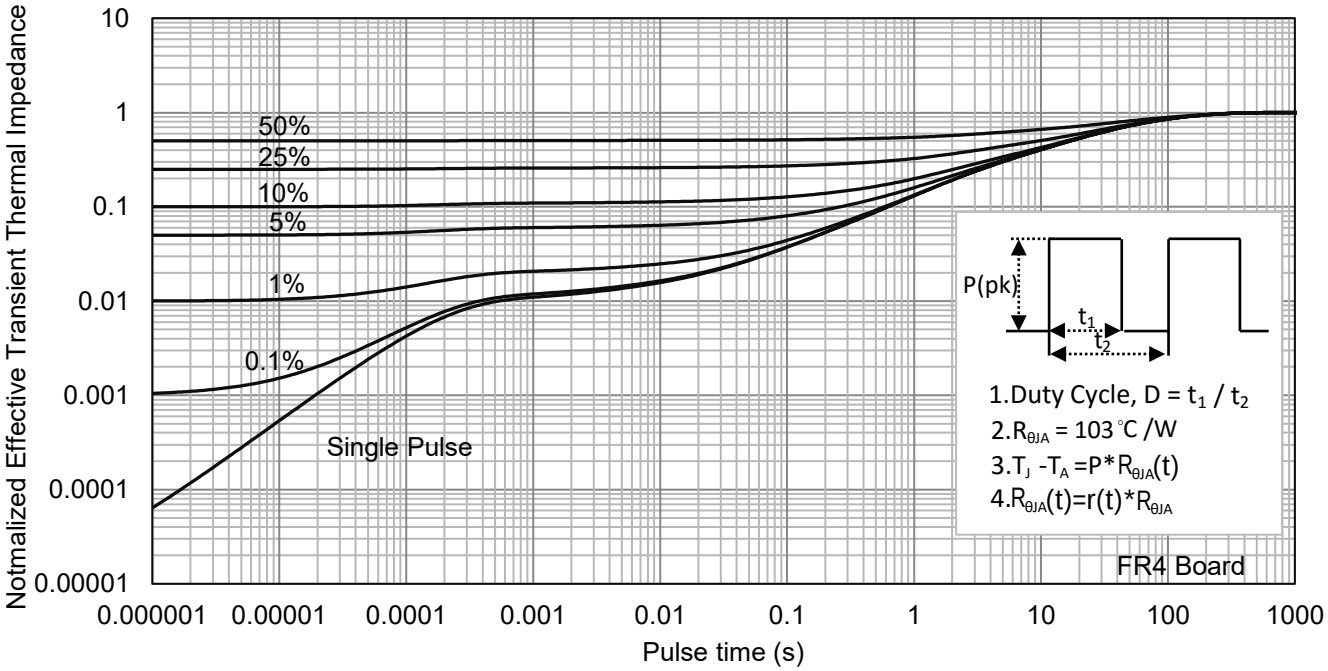


Capacitance

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



Safe Operating Area



Thermal Response

8.OUTLINE AND DIMENSIONS

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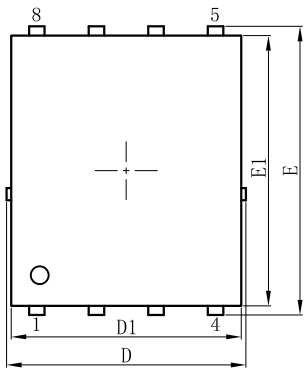
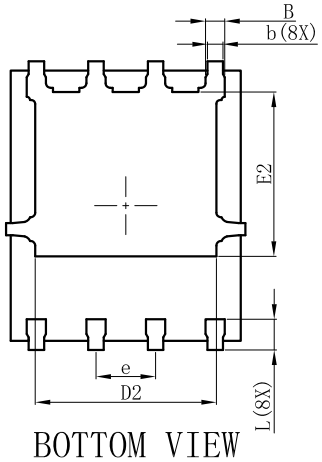
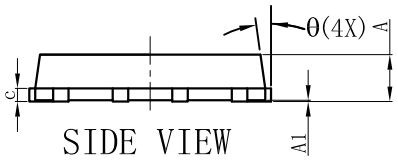


TOP VIEW



BOTTOM VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

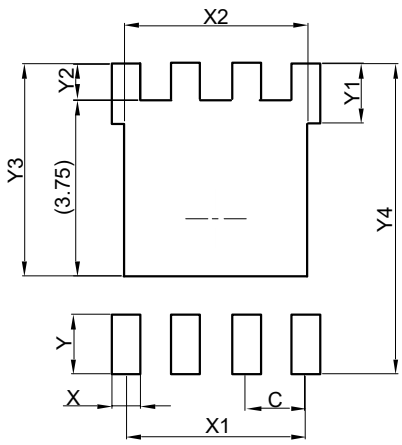


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61