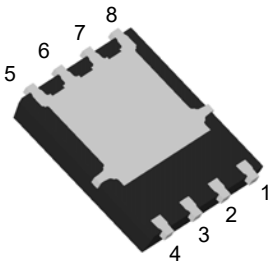
# N7460D

60V N-Channel MOSFET



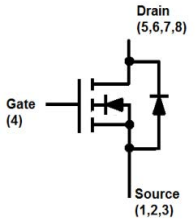

DFN5060-8B

## 1. FEATURES

- 60V,104A, RDS(ON) ≤2.5mΩ@VGS = 10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

## 2. APPLICATIONS

- Networking
- Load Switch
- LED applications




## 3. DEVICE MARKING AND RESISTOR VALUES

| Device | Marking | Shipping |
|---|---|---|
| N7460D | LN7460 | 3000/Tape&Reel |

## 4. MAXIMUM RATINGS(Ta = 25ºC)

| Parameter | | Symbol | Limits | Unit |
|---|---|---|---|---|
| Drain-to-Source Voltage | | VDS | 60 | V |
| Gate-to-Source Voltage | | VGS | ±20 | V |
| Continuous Drain Current | TC=25℃ | ID | 104 | A |
| | TC=100℃ | | 80 | A |
| | TA=25℃ | | 28 | A |
| | TA=100℃ | | 21 | A |
| Pulsed Drain Current(Note 1) | | IDM | 112 | A |
| Avalanche Current(L=0.1mH) | | IAS | 45 | A |
| Avalanche Energy(L=0.1mH) | | EAS | 101 | mJ |
| Power Dissipation | TC=25℃ | PD | 35 | W |
| | TA=25℃ | | 2.5 | W |
| Operating Junction and Storage Temperature Range | | Tj/Tstg | -50~+150 | ℃ |

## 5. THERMAL CHARACTERISTICS

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Maximum Junction-to-Ambient(Note 2) | RθJA | 50 | ℃/W |
| Maximum Junction-to-Case | RθJC | 3.5 | |

1.Repetitive Rating : Pulsed width limited by maximum junction temperature.

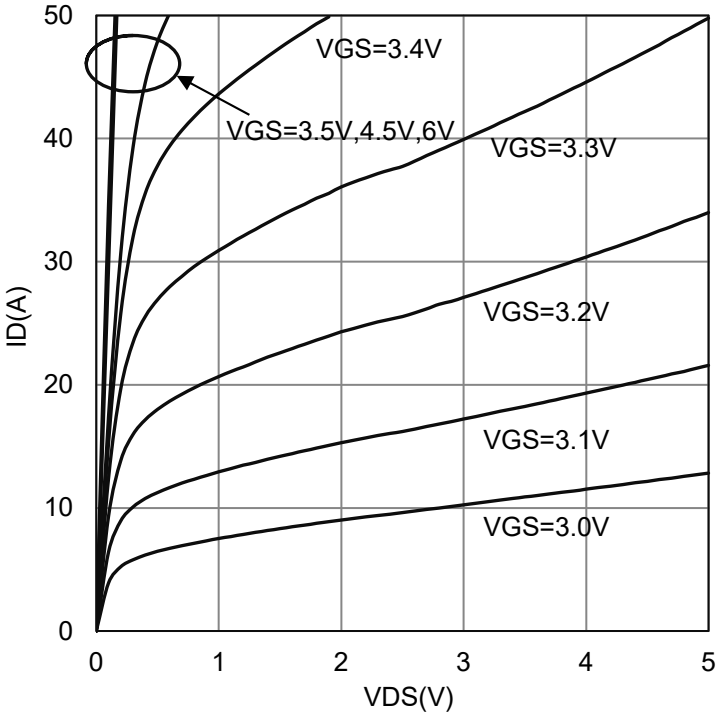
2.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu

## 6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

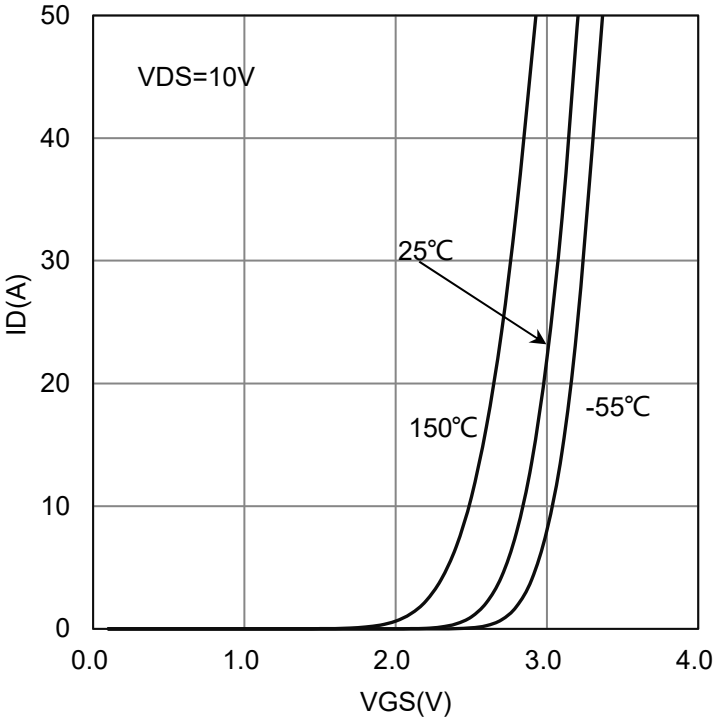
| Characteristic | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Static | | | | | | |
| Drain to Source Breakdown Voltage (VGS =0V, ID =250μA) | | VDSS | 60 | - | - | V |
| Drain-to-Source Leakage Current (VDS =60V,VGS =0V) | | IDSS | - | - | 1 | μA |
| Gate-Body leakage current (VDS =0V, VGS = ±20V) | | IGSS | - | - | ±100 | nA |
| Gate Threshold Voltage (VDS = VGS , ID = 250μA) | | VGS(TH) | 1.2 | 1.7 | 2.5 | V |
| Drain-to-Source On-Resistance(Note 3)<br>(VGS =10V,ID =20A)<br>(VGS =4.5V,ID =10A) | | RDS(ON) | -<br>- | 2<br>2.8 | 2.5<br>3.3 | mΩ |
| Dynamic | | | | | | |
| Total Gate Charge | (VDS =30V,VGS =10V,ID =50A) | Qg | - | 113 | - | nC |
| Gate to Source Charge | | Qgs | - | 20 | - | |
| Gate to Drain Charge | | Qgd | - | 31.5 | - | |
| Turn-on Delay Time | (VDD =15V,VGS =10V,RG =3.3Ω,ID =1A) | td(ON) | - | 19 | - | nS |
| Rise Time | | tr | - | 12 | - | |
| Turn-Off Delay Time | | td(OFF) | - | 62 | - | |
| Fall Time | | tf | - | 130 | - | |
| Input Capacitance | (VDS =30V,VGS =0V,F=1MHz) | Ciss | - | 4984 | - | pF |
| Output Capacitance | | Coss | - | 1798 | - | |
| Reverse Transfer Capacitance | | Crss | - | 102.8 | - | |
| Internal Gate Resistance | | Rg | - | 1.1 | - | Ω |
| Diode Forward Voltage (VGS =0V,IS =1A,TJ =25℃) | | VSD | - | - | 1 | V |
| Continuous Source Current (VG =VD =0V , Force Current) | | IS | - | - | 28 | A |
| Pulsed Source Current (VG =VD =0V , Force Current) | | ISM | - | - | 112 | A |
| Reverse Recovery Time | (VGS=10V,IS= 10A,di/dt=100 A/μs,TJ=25℃) | trr | - | 88 | - | ns |
| Reverse Recovery Charge | | Qrr | - | 175 | - | nC |

3.Pulse test: PW≤ 300μs duty cycle ≤ 2%.

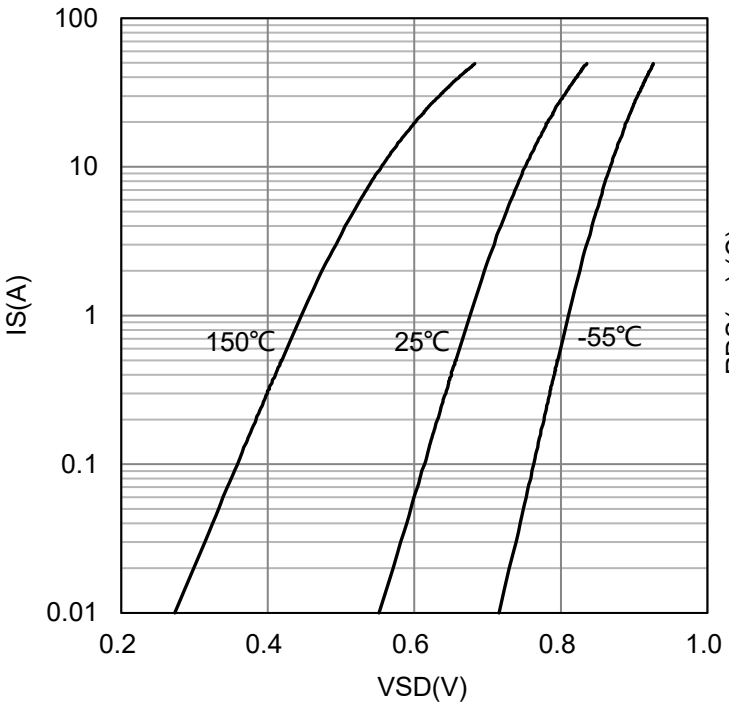
## 7.ELECTRICAL CHARACTERISTICS CURVES



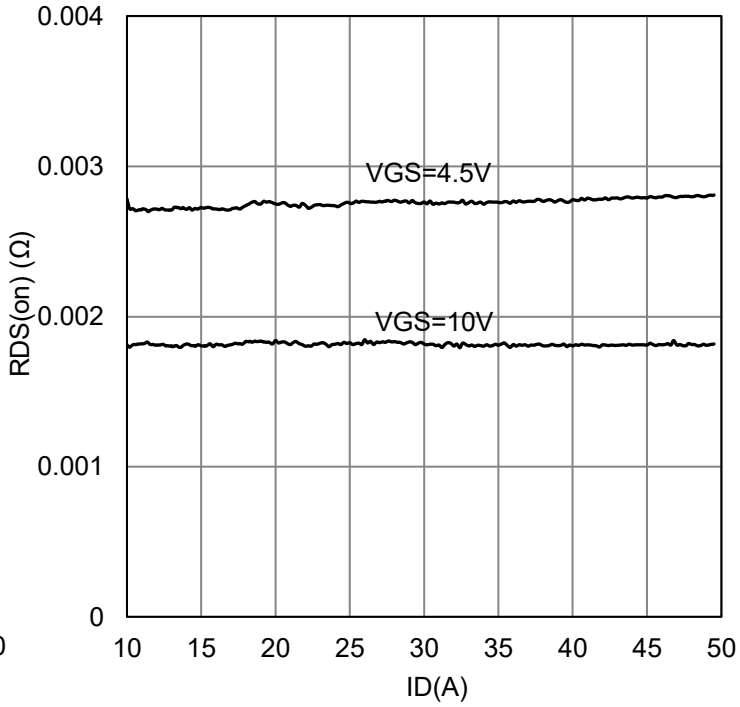

ID vs. VDS




ID vs. VGS

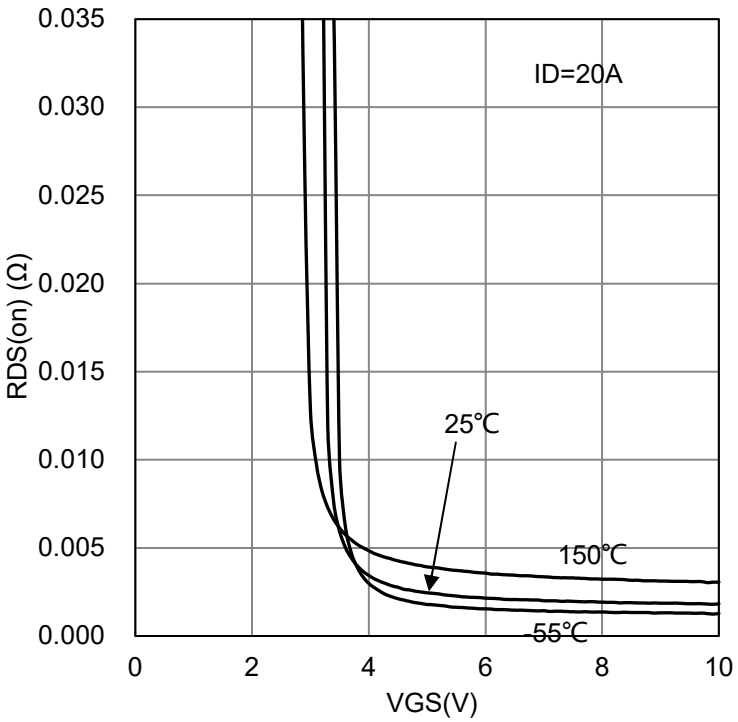



IS vs. VSD

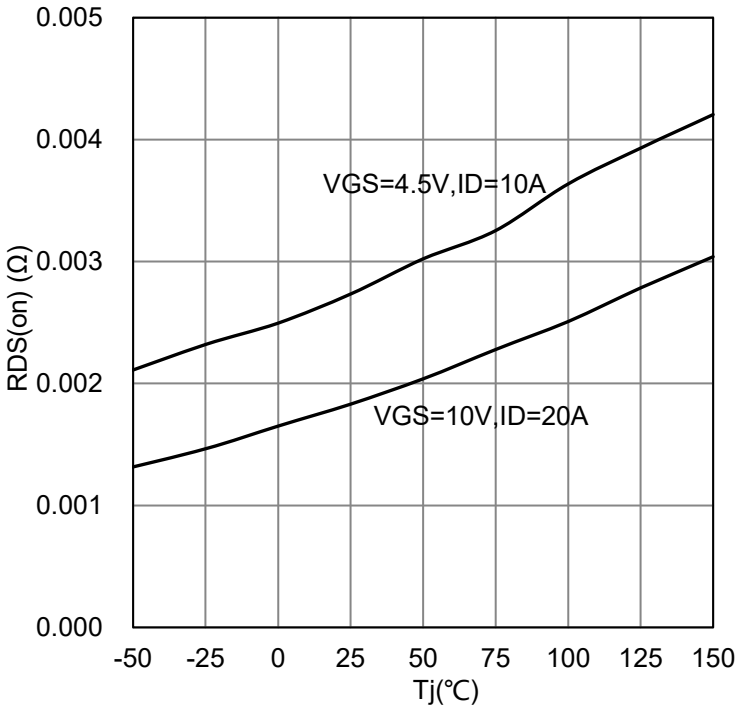



RDS(on) vs. ID

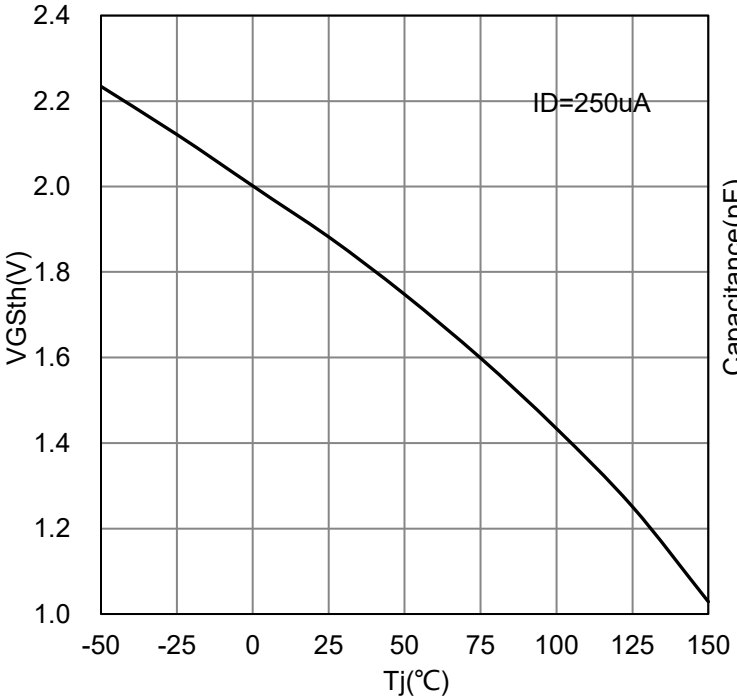
## 7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



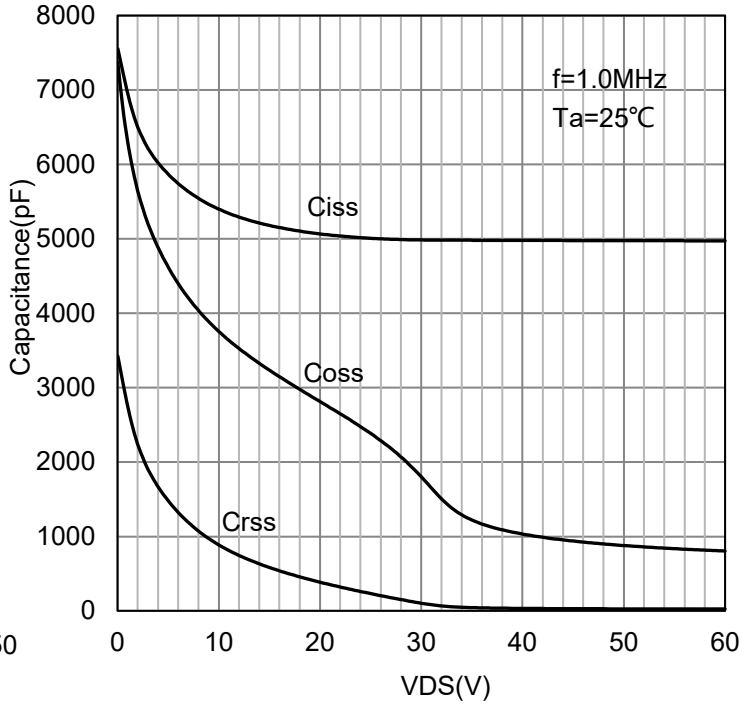

RDS(on) vs. VGS




RDS(on) vs. Tj




VGSth vs. Tj




Capacitance

## 8.OUTLINE AND DIMENSIONS

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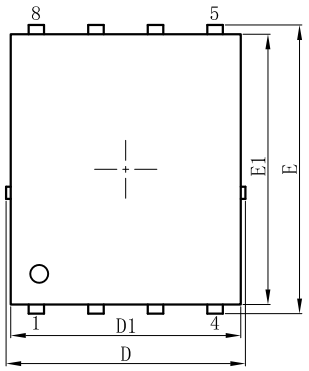
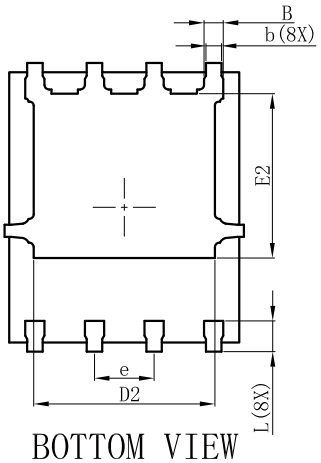
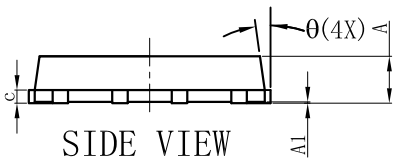



TOP VIEW




BOTTOM VIEW

| DFN5060-8B | | | |
|---|---|---|---|
| DIM | MIN | NOR | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | 0.02 | 0.05 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.66 | 5.76 | 5.86 |
| E2 | 3.40 | 3.50 | 3.60 |
| D | 4.95 | 5.10 | 5.25 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.76 | 3.86 | 3.96 |
| b | 0.30 | 0.35 | 0.40 |
| B | 0.36 | 0.41 | 0.46 |
| L | 0.56 | 0.66 | 0.76 |
| e | 1.27BSC | | |
| c | 0.254REF. | | |
| θ | 0° | - | 12° |
| All Dimensions in mm | | | |

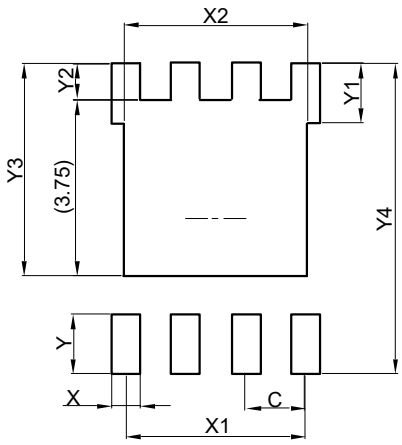



SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

## 9.SOLDERING FOOTPRINT




| DFN5060-8B | |
|---|---|
| DIM | (mm) |
| C | 1.27 |
| X | 0.61 |
| X1 | 3.81 |
| X2 | 3.91 |
| Y | 1.27 |
| Y1 | 1.27 |
| Y2 | 0.77 |
| Y3 | 4.52 |
| Y4 | 6.61 |