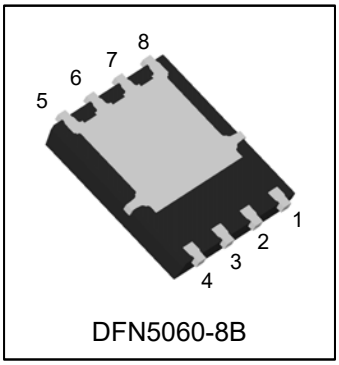
N7402D

N-Channel 40-V (D-S) MOSFET



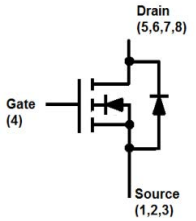
DFN5060-8B

1. FEATURES

- Low RDS(on) trench technology
- Low thermal impedance
- Fast switching speed
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

2. APPLICATIONS

- DC/DC Conversion
- Power Routing
- Motor Drives



3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
N7402D	LN7402	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		VDSS	40	V
Gate−to−Source Voltage		VGS	±20	V
Continuous Drain Current	TC =25°C	ID	104	A
	TC =70°C		92	
	TA =25°C		28	
	TA =70°C		24	
Pulsed Drain Current (Note 2)		IDM	112	
Avalanche Current		IAS	40	A
Avalanche energy (L=0.3mH)		EAS	80	mJ
Power Dissipation	TC =25°C	PD	35	W
	TC =70°C		27	
	TA =25°C		2.5	
	TA =70°C		1.9	
Operating Junction Temperature		TJ	−55 ~+150	℃
Storage Temperature Range		Tstg	−55 ~+150	

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Junction-to-Ambient(Note 2)	RθJA	50	℃/W
Maximum Junction-to-Case	RθJC	3.5	

1.Repetitive Rating : Pulsed width limited by maximum junction temperature.
2.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu

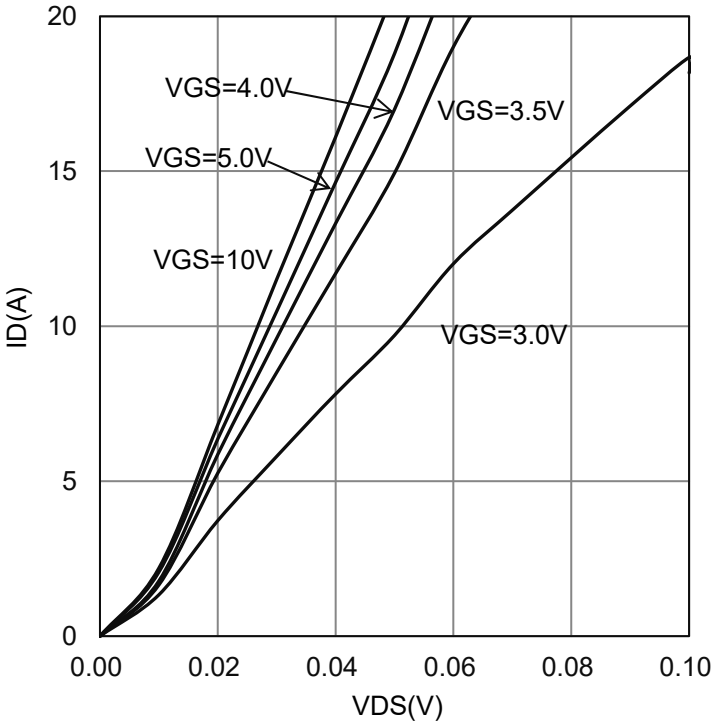
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = 250μA)		VBRDSS	40	-	-	V
Gate Threshold Voltage (VDS = VGS , ID = 250 uA)		VGS(TH)	1	-	3	V
Gate-Body leakage current (VDS =0V, VGS = ±20V)		IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VDS = 32 V, VGS = 0 V) (VDS = 32 V, VGS = 0 V, TJ = 55°C)		IDSS	- -	- -	1 10	μA
Drain-to-Source On-Resistance (Note 3) (VGS = 10 V, ID = 20 A) (VGS = 4.5 V, ID = 16 A)		RDS(ON)	- -	- -	2.0 2.5	mΩ
Diode Forward Voltage (IS = 5 A, VGS = 0 V)		VSD	-	0.7	-	V
Dynamic(Note 4)						
Total Gate Charge	(VDS = 20 V, VGS = 4.5 V,ID = 20 A)	Qg	-	56.8	-	nC
Gate to Source Charge		Qgs	-	17	-	
Gate to Drain Charge		Qgd	-	21.6	-	
Turn-on Delay Time	(VDS=20 V,RL =1Ω,ID=20 A,VGEN=10 V, RGEN=6 Ω)	td(on)	-	30	-	nS
Rise Time		tr	-	47	-	
Turn-Off Delay Time		td(off)	-	311	-	
Fall Time		tf	-	100	-	
Input Capacitance	(VDS = 15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	6092	-	pF
Output Capacitance		Coss	-	1498	-	
Reverse Transfer Capacitance		Crss	-	308	-	
Gate-Resistance (VDS=0V,VGS=0V,f=1.0MHz)		Rg	-	2	-	Ω

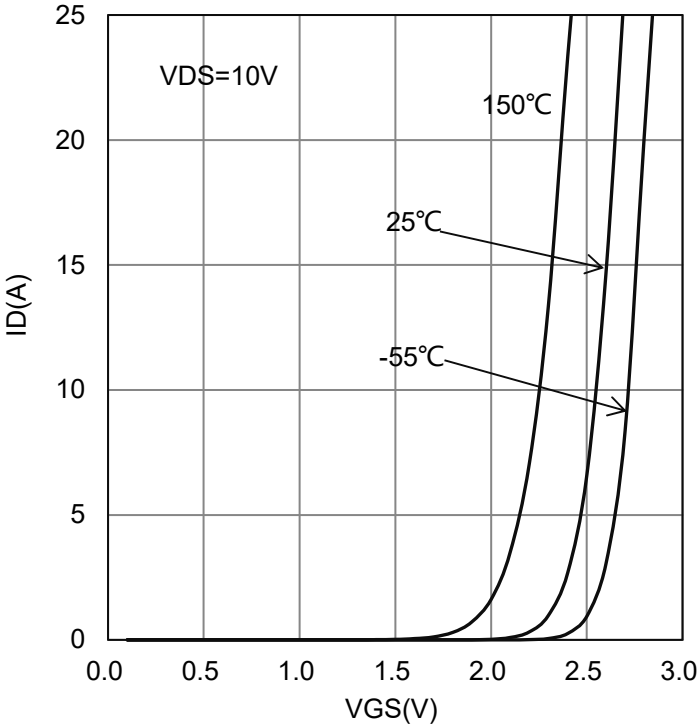
3.Pulse test: PW ⩽ 300μs duty cycle ⩽ 2%.

4.Guaranteed by design, not subject to production testing.

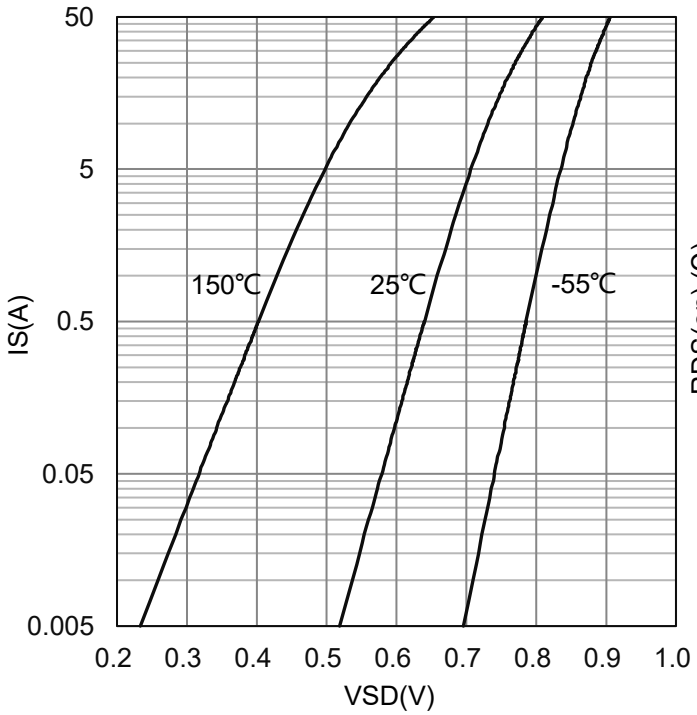
7.ELECTRICAL CHARACTERISTICS CURVES



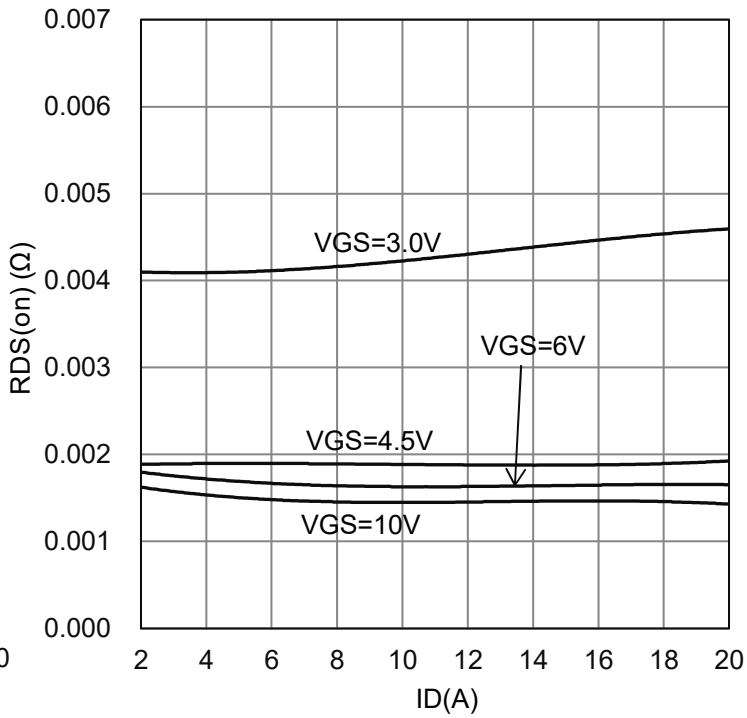
ID vs. VDS



ID vs. VGS

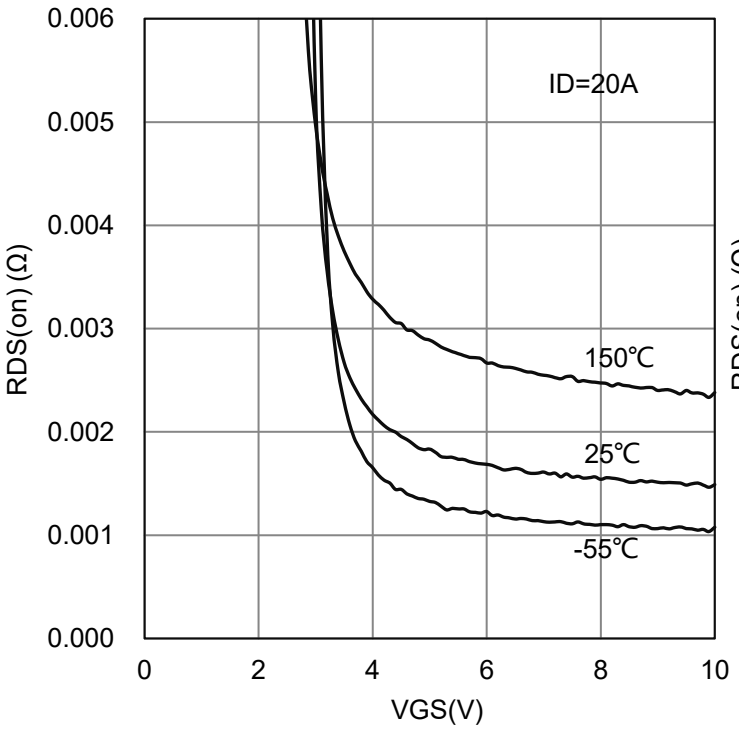


IS vs. VSD

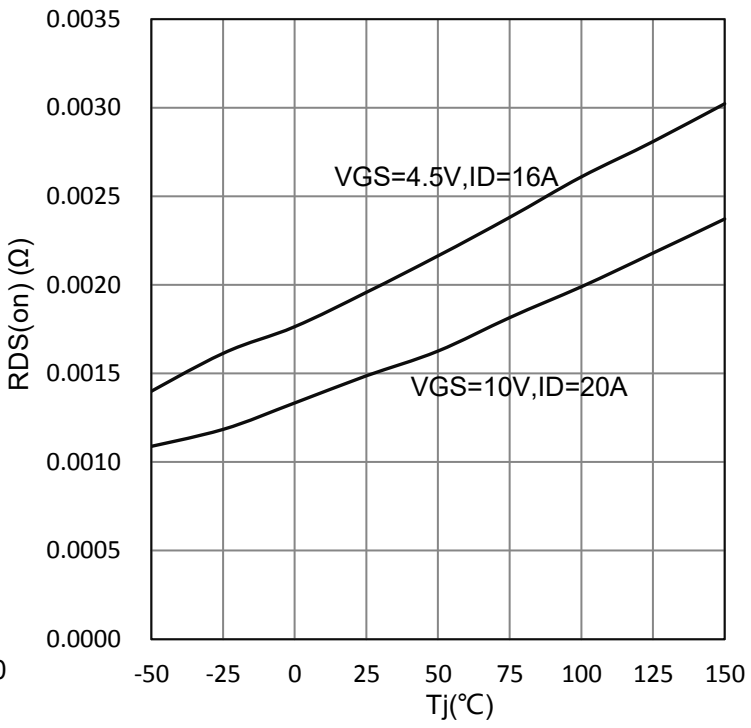


RDS(on) vs. ID

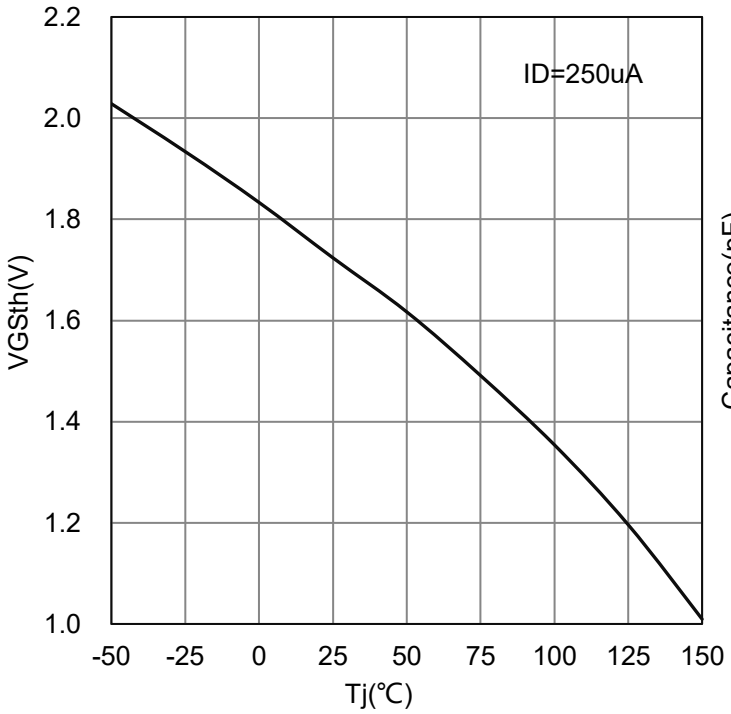
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



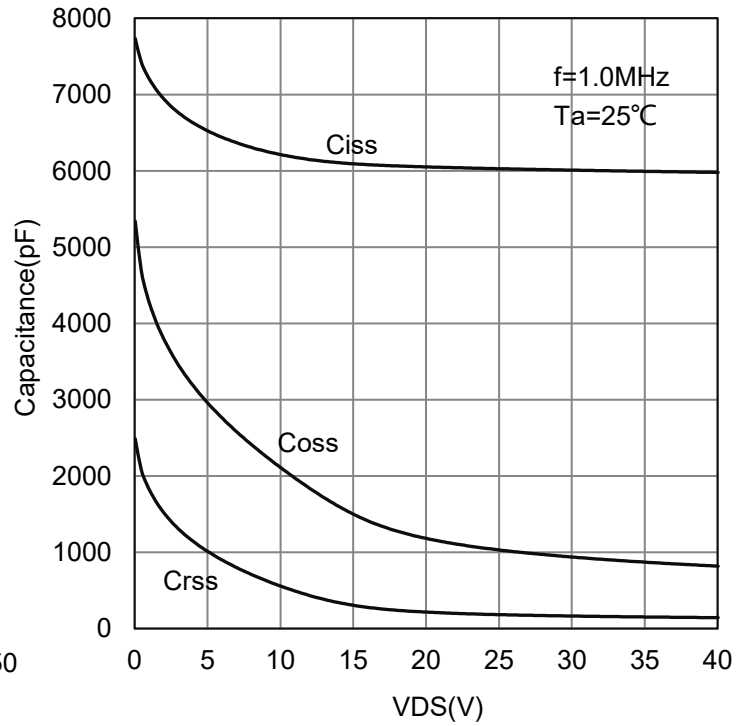
RDS(on) vs. VGS



RDS(on) vs. Tj



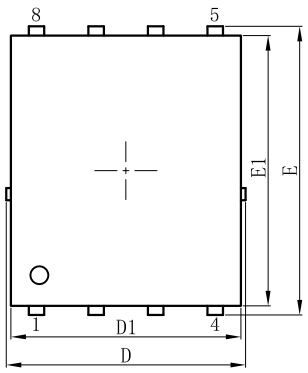
VGSth vs. Tj



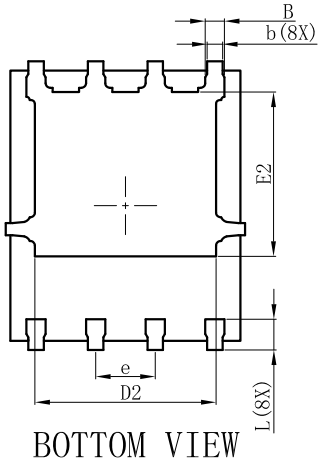
Capacitance

8.OUTLINE AND DIMENSIONS

DFN5060-8B

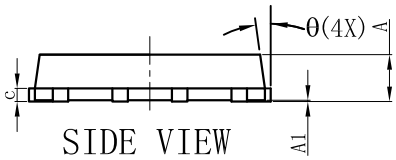


TOP VIEW



BOTTOM VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

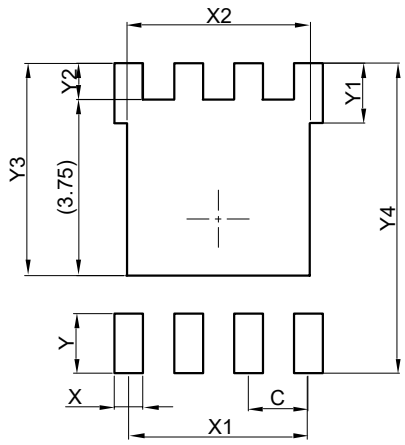


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61