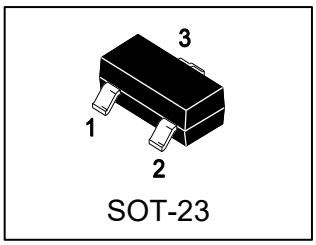
N2312

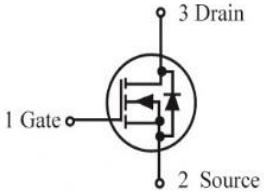
20V N-Channel Enhancement-Mode MOSFET

1. FEATURES



- VDS= 20V
- RDS(ON), VGS@4.5V, IDS@5A ≤ 41mΩ
- RDS(ON), VGS@2.5V, IDS@4.5A ≤ 47mΩ
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

2. APPLICATIONS



- High density cell design for ultra low on-resistance
- Advanced trench process technology

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
N2312	N12	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	20	V
Gate–to–Source Voltage – Continuous	VGS	±8	V
Drain Current – Continuous TA = 25°C – Pulsed(Note 1)	 ID IDM	 4.9 15	A

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	0.75	W
Thermal Resistance, Junction–to–Ambient(Note 2)	RΘJA	140	ºC/W
Junction and Storage temperature	TJ,Tstg	−55~+150	° C

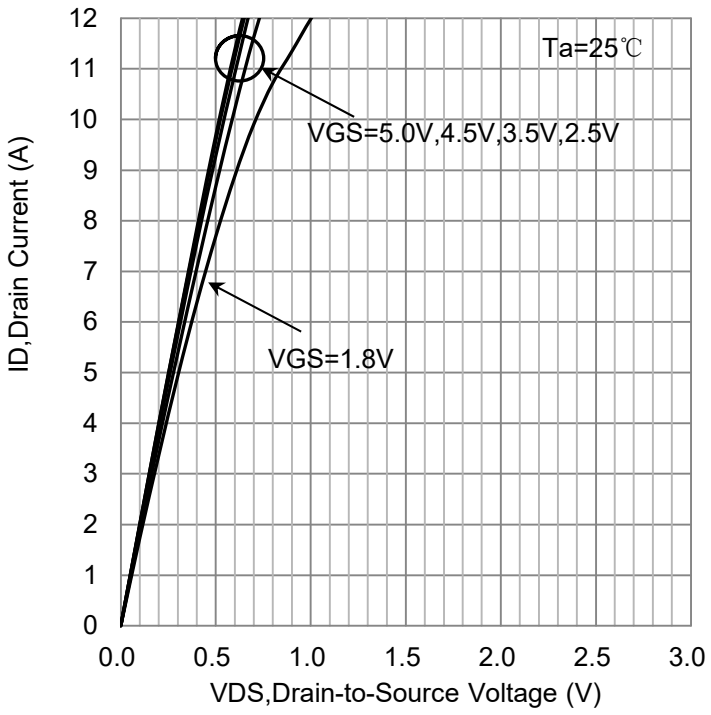
1. Repetitive Rating: Pulse width limited by the Maximum junction temperation.
2. 1-in² 2oz Cu PCB board.

6. ELECTRICAL CHARACTERISTICS (Ta= 25℃)

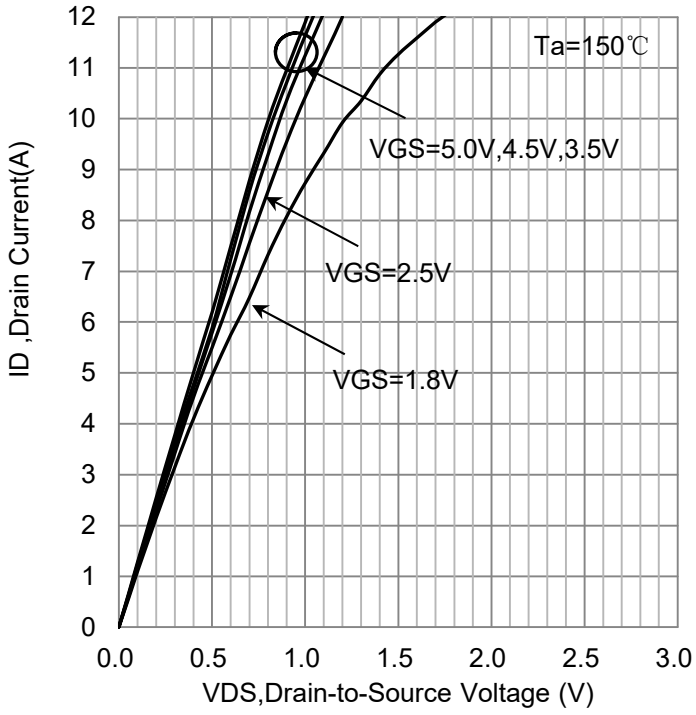
Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain–Source Breakdown Voltage (VGS = 0, ID = 250μA)		V(BR)DSS	20	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = 250μA)		VGS(th)	0.4	0.6	1.0	V
Zero Gate Voltage Drain Current (VDS=20V, VGS=0V)		IDSS	-	-	1	μA
Gate–Body Leakage Current, Forward (VDS = 0 V, VGS = 8 V)		IGSSF	-	-	100	nA
Gate–Body Leakage Current, Reverse (VDS = 0 V, VGS = -8 V)		IGSSR	-	-	-100	nA
Static Drain–Source On–State Resistance (VGS = 1.8 V, ID = 4 A) (VGS = 2.5 V, ID = 4.5 A) (VGS = 4.5 V, ID = 5 A)		RDS(on)	- - -	31 24 21	57 47 41	mΩ
Diode Forward Voltage (VGS = 0 V, ISD = 1.7 A)		VSD	-	-	1.2	V
DYNAMIC						
Input capacitance	(VDS =8V, VGS =0V, f=1MHz)	Ciss	-	500	-	pF
Output Capacitance		Coss	-	300	-	
Reverse Transfer Capacitance		Crss	-	140	-	
Turn-On Delay Time	(VDD =10V, ID =1A, VGEN=4.5V, RG = 6Ω)	td(on)	-	5.5	-	ns
Rise Time		tr	-	10	-	
Turn-Off Delay Time		td(off)	-	33	-	
Fall Time		tf	-	15	-	
Total Gate Charge	(VDS = 10 V, VGS = 4.5 V,ID = 5 A)	Qg	-	5.9	-	nC
Gate to Source Charge		Qgs	-	0.9	-	
Gate to Drain Charge		Qgd	-	1.3	-	

3.Pulse test; pulse width≤300μs, duty cycle≤2%.

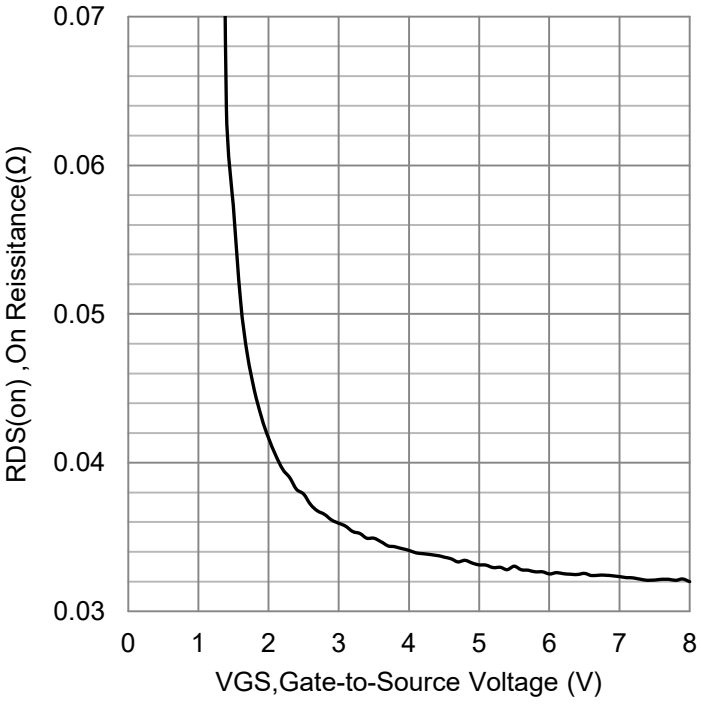
7. ELECTRICAL CHARACTERISTICS CURVES



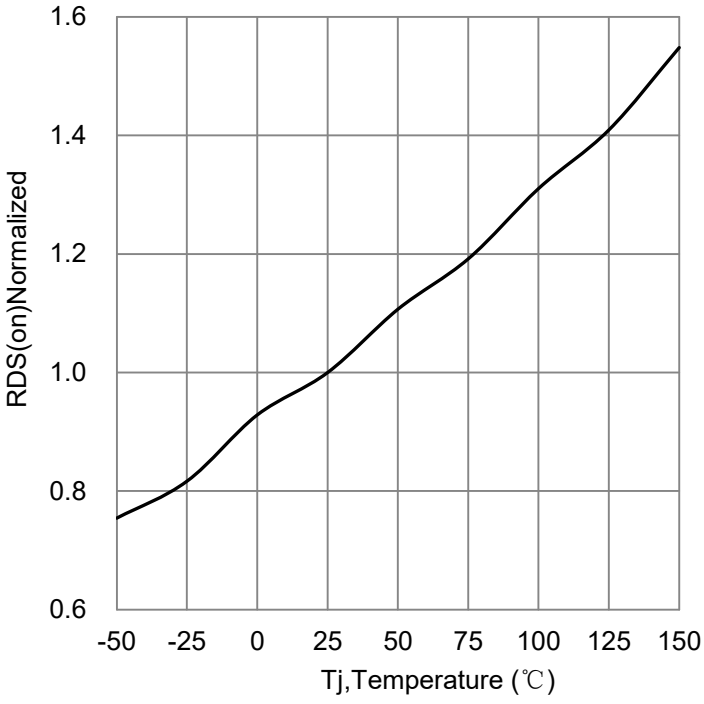
Typical Output Characteristics



Typical Output Characteristics

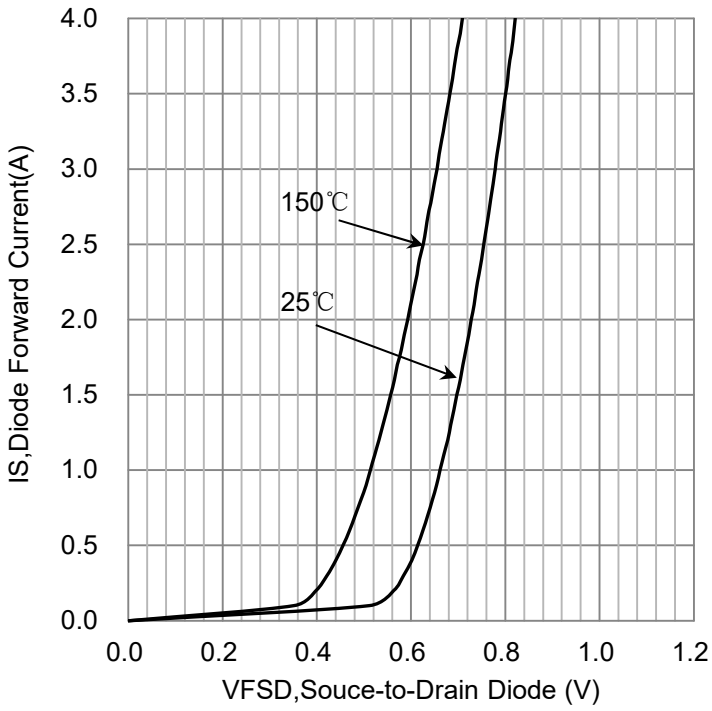


RDS(on) vs. VGS

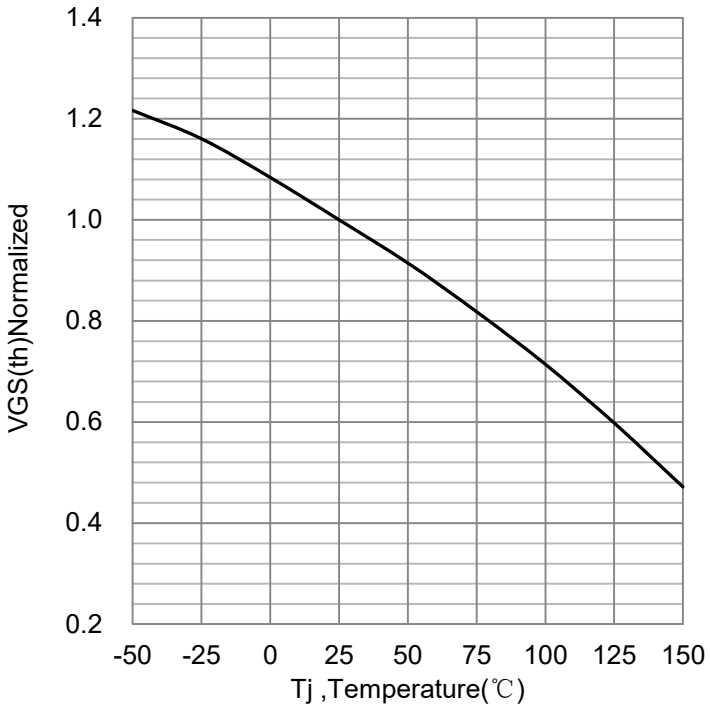


RDS(on) vs. Tj

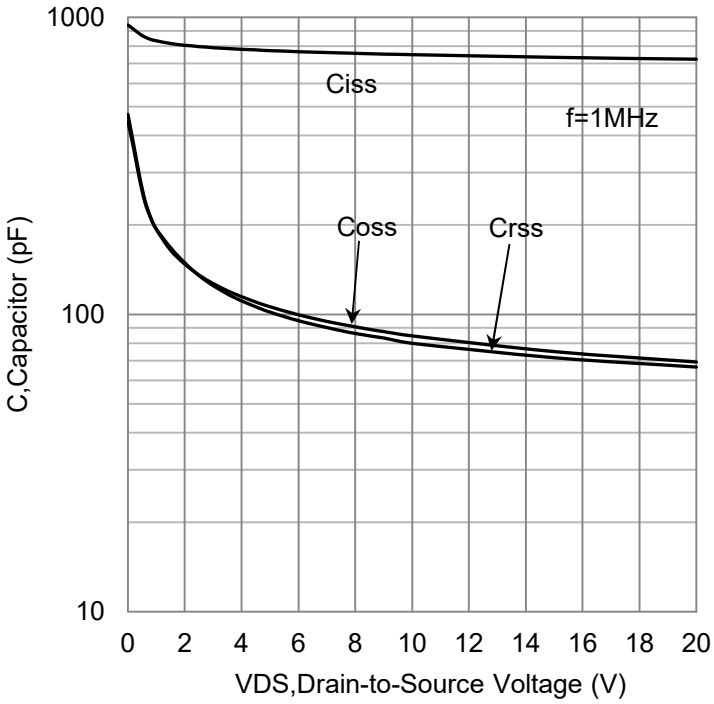
7. ELECTRICAL CHARACTERISTICS CURVES（Con.）



Forward Characteristic of Reverse Diode

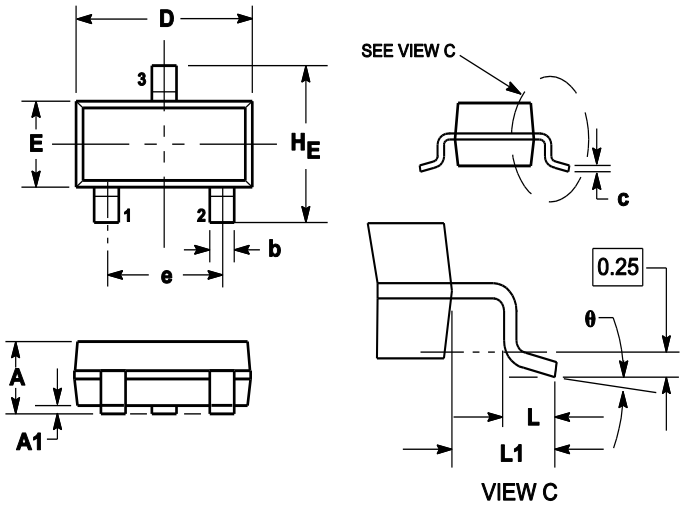


VGS(th) vs. Tj



Typical Capacitance Characteristics

8.OUTLINE AND DIMENSIONS



Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9.SOLDERING FOOTPRINT