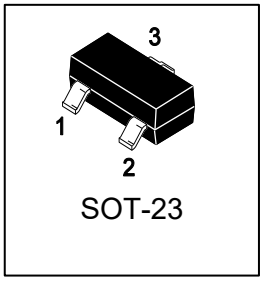
N2308EL
S-N2308EL

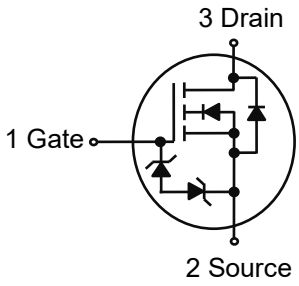
60V N-Channel Power MOSFET



SOT-23

1. FEATURES

- Gate to Source ESD Protected
- Super high density cell design for extremely low RDS(ON).
- Exceptional on-resistance and maximum DC current capability.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.



2. APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
N2308EL	E08	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	VDSS	60	V
Gate–to–Source Voltage – Continuous	VGS	±20	V
Drain Current – Continuous TA = 25°C – Continuous TA = 70°C	ID	 2.6 2	A
– Pulsed(Note 1)	IDM	10.4	
Junction and Storage temperature	TJ,Tstg	-55~+150	℃

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	0.9	W
Thermal Resistance, Junction–to–Ambient(Note 2) Junction–to–Case	 RθJA RθJC	 140 105	℃/W

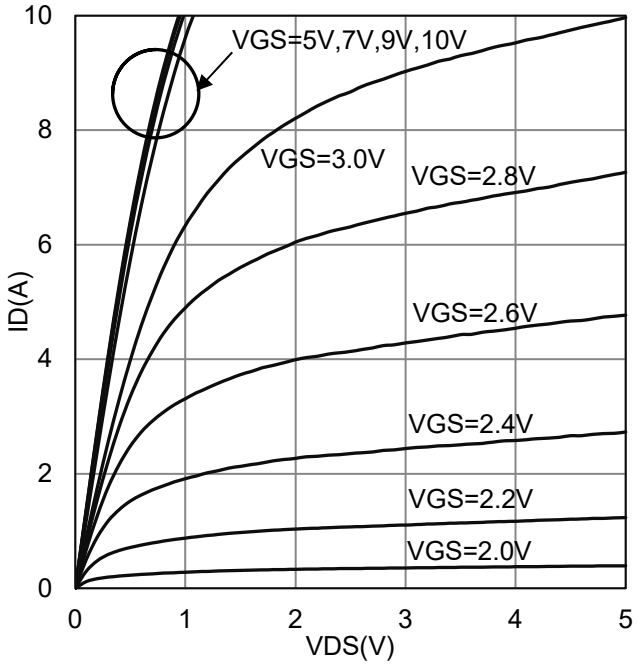
1. Repetitive Rating: Pulse width limited by the Maximum junction temperation.
2. 1-in² 2oz Cu PCB board.

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

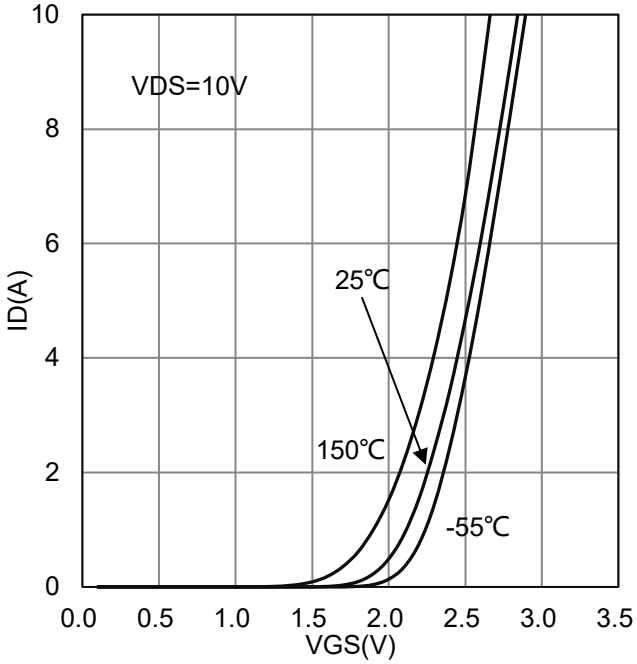
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = 250μA)		V(BR)DSS	60	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = 250μA)		VGS(th)	1	1.5	2.5	V
Gate Body Leakage (VDS =0V, VGS =±20V)		IGSS	-	-	±10	μA
Zero Gate Voltage Drain Current (VDS =48V, VGS =0V)		IDSS	-	-	1	μA
Static Drain–Source On–State Resistance (VGS = 10 V, ID = 2 A) (VGS = 4.5 V, ID = 2 A)		RDS(on)	- -	- -	100 120	mΩ
Diode Forward Voltage (IS =0.5A, VGS =0V)		VSD	-	0.7	1.3	V
Dynamic						
Total Gate Charge	(VDS =30V, VGS =4.5V, ID =2A)	Qg	-	3.3	-	nC
Gate-Source Charge		Qgs	-	0.7	-	
Gate-Drain Charge		Qgd	-	1.4	-	
Input capacitance	(VDS =30V, VGS =0V, f=1MHz)	Ciss	-	312	-	pF
Output Capacitance		Coss	-	20	-	
Reverse Transfer Capacitance		Crss	-	16	-	
Turn-On Delay Time	(VDD =30V, RL =30Ω,ID =1A, VGEN =10V,RG =3Ω)	td(on)	-	3.6	-	ns
Turn-On Rise Time		tr	-	10.2	-	
Turn-Off Delay Time		td(off)	-	17.1	-	
Turn-Off Fall Time		tf	-	11	-	
Gate Resistance (VDS=0V ,VGS=0V, f=1.0MHz)		Rg	-	4.8	-	Ω

3.Pulse test; pulse width≤300μs, duty cycle≤2%.

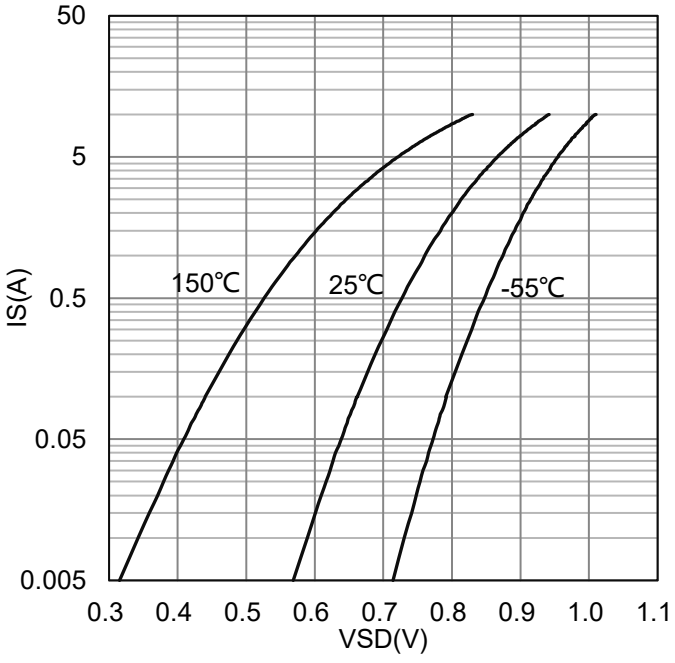
7. ELECTRICAL CHARACTERISTICS CURVES



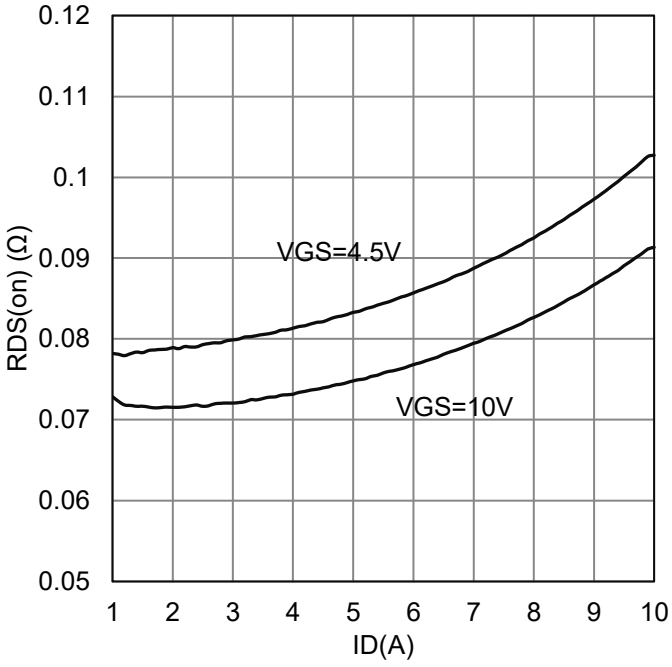
ID vs. VDS



ID vs. VGS

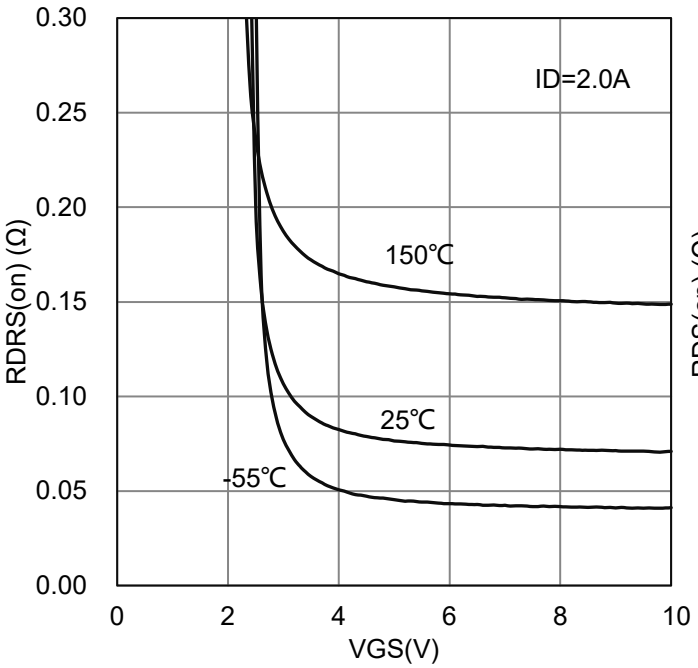


IS vs. VSD

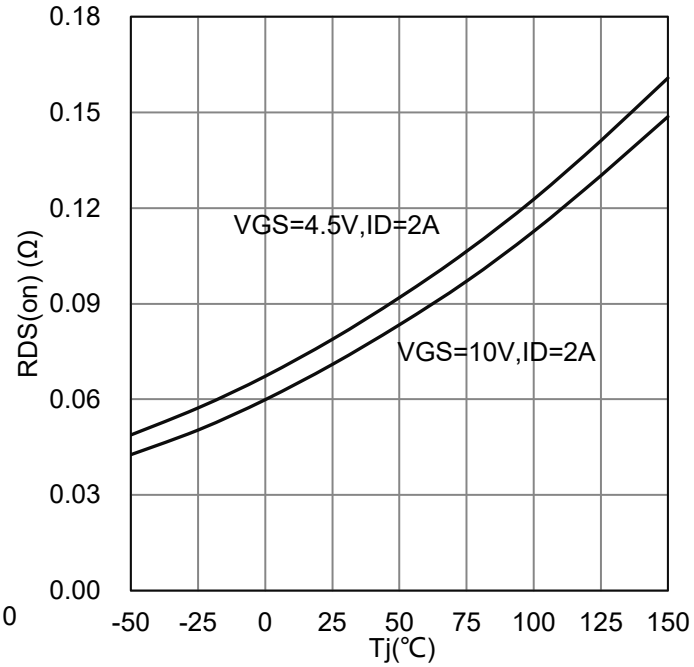


RDS(on) vs. ID

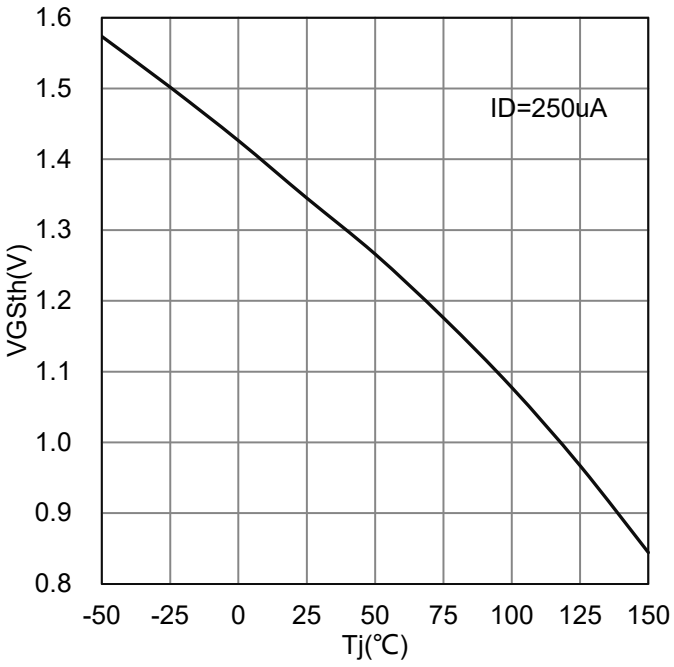
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



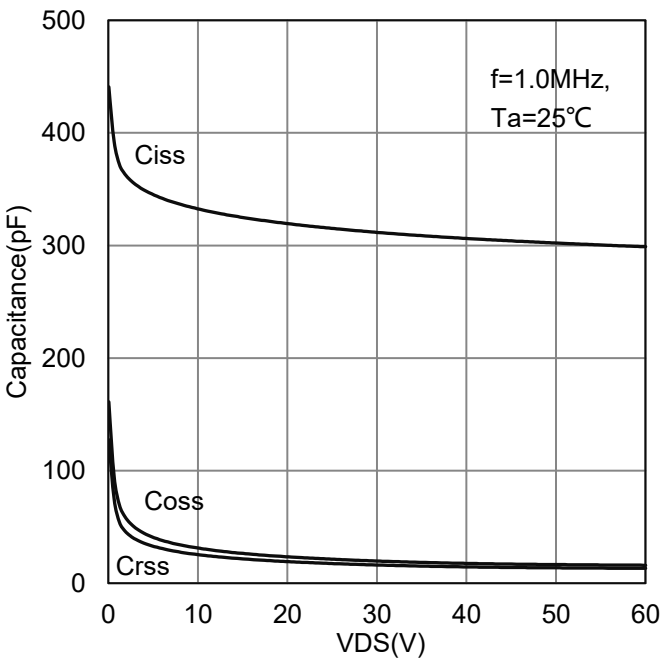
RDS(on) vs. VGS



RDS(on) vs. Tj

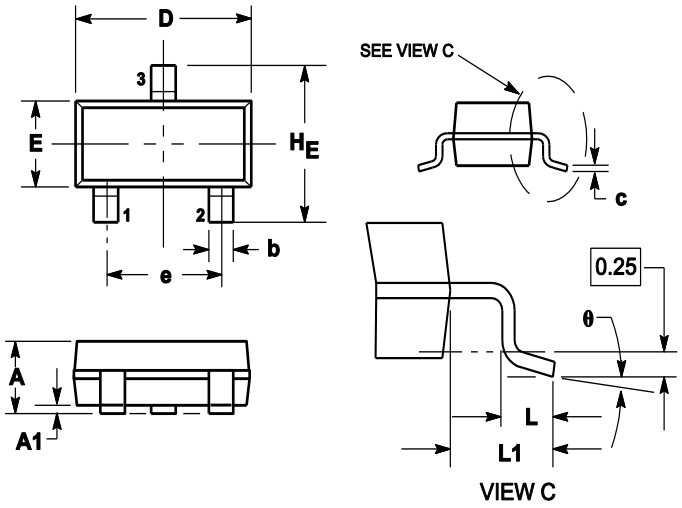


VGSth vs. Tj



Capacitance

8.OUTLINE AND DIMENSIONS



Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9.SOLDERING FOOTPRINT