

2N7002FL

S-2N7002FL

Small Signal MOSFET
30V N-Channel SOT-23

1. FEATURES

- $R_{DS(ON)} \leq 8\Omega, V_{GS@4V}$
 $R_{DS(ON)} \leq 13\Omega, V_{GS@2.5V}$
- ESD Protected:1000V
- Super high density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

2. APPLICATIONS

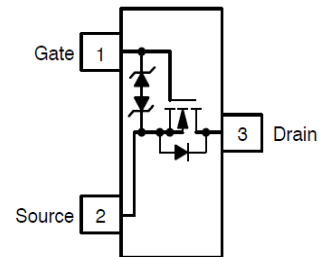
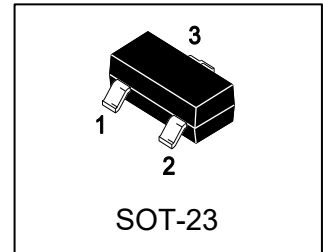
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
2N7002FL	72F	3000/Tape&Reel

4. MAXIMUM RATINGS($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current(Steady State)	I _D	115	mA



5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Total Device Dissipation, FR-5 Board (Note 1) @ TA = 25°C Derate above 25°C	PD	225 1.8	mW mW/°C
Thermal Resistance, Junction-to-Ambient(Note 1)	RθJA	556	°C/W
Total Device Dissipation, Alumina Substrate (Note 2) @ TA = 25°C Derate above 25°C	PD	300 2.4	mW mW/°C
Thermal Resistance, Junction-to-Ambient(Note 2)	RθJA	417	°C/W
Junction and Storage temperature	TJ,Tstg	-55~+150	°C

1. FR-5 = 1.0×0.75×0.062 in.

2. Alumina=0.4×0.3×0.025 in 99.5% alumina.



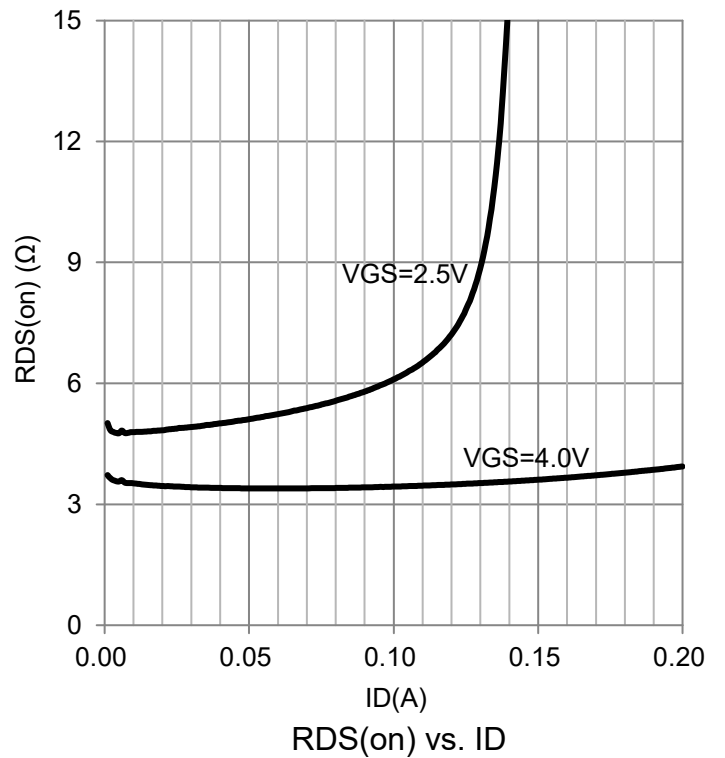
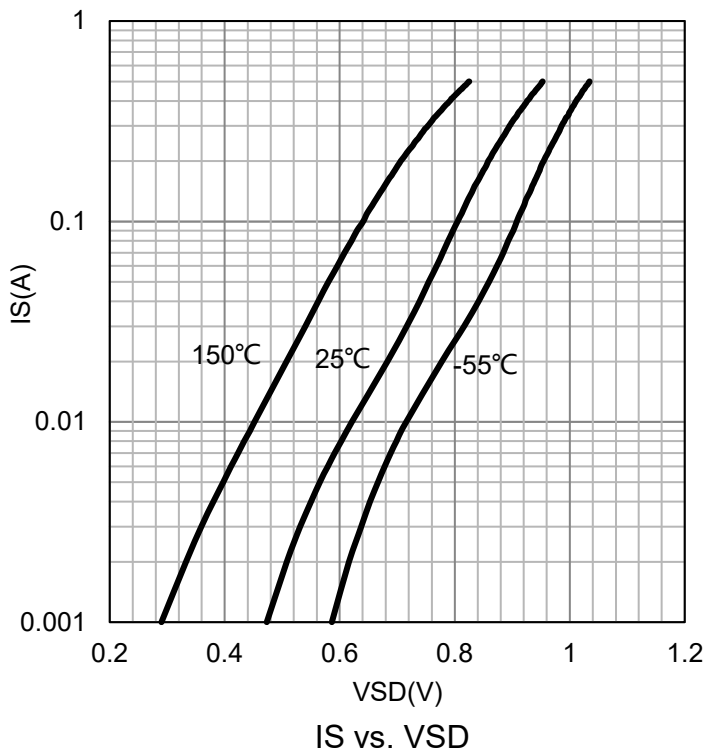
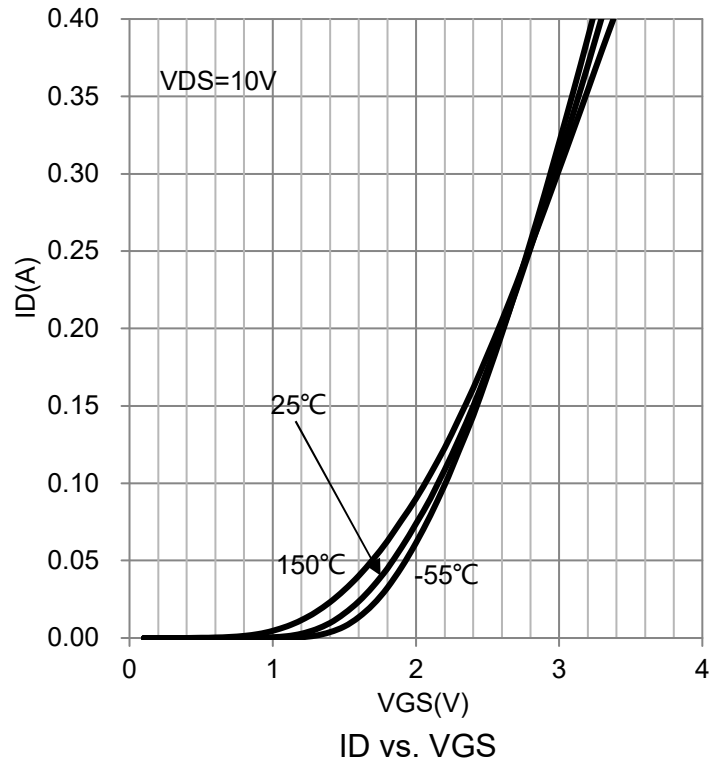
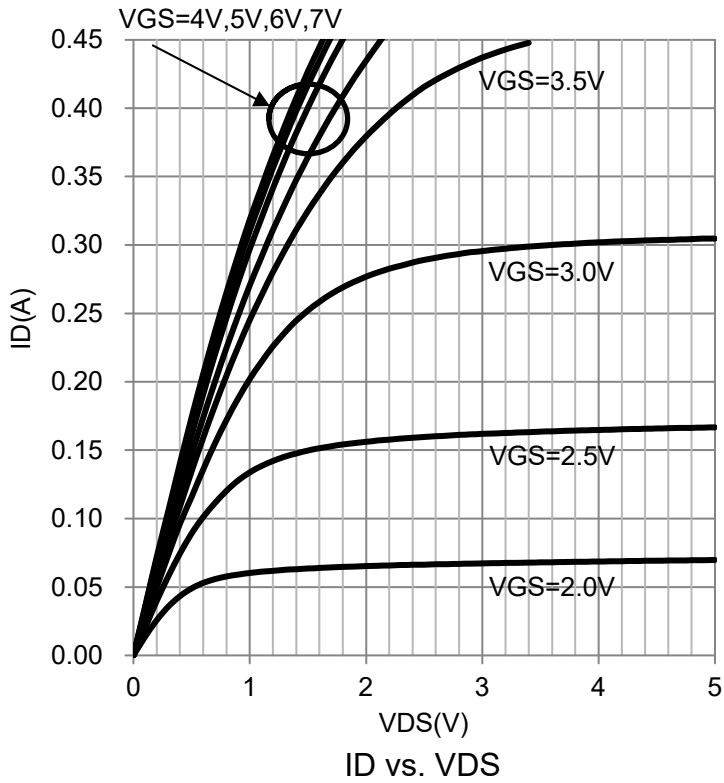
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	
STATIC						
Drain–Source Breakdown Voltage (VGS = 0, ID = 250μA)	VBRDSS	30	-	-	V	
Gate Threshold Voltage (VDS = VGS, ID = 250μA)	VGS(th)	0.8	-	1.5	V	
Gate–Body Leakage Current (VGS = ±20V, VDS=0V)	IGSS	-	-	±10	μA	
Zero Gate Voltage Drain Current (VGS = 0, VDS = 30 V)	IDSS	-	-	1	μA	
Static Drain–Source On–State Resistance (VGS = 4 V, ID = 10 mA) (VGS = 2.5 V, ID = 1 mA)	RDS(on)	-	5 7	8 13	Ω	
Diode Forward Voltage (IS = 200 mA, VGS = 0 V)	VSD	-	-	1.2	V	
DYNAMIC						
Total Gate Charge	(VDS =25V, VGS =10V, ID =0.22A)	Qg	-	4.9	-	nC
Gate-Source Charge		Qgs	-	2.1	-	
Gate-Drain Charge		Qgd	-	0.6	-	
Input capacitance	(VDS =25V, VGS =0V, f=1MHz)	Ciss	-	21	-	pF
Output Capacitance		Coss	-	10	-	
Reverse Transfer Capacitance		Crss	-	2	-	
Turn-On Delay Time	(VDD =5V, RL =500Ω, VGES =5V, RG =10Ω)	td(on)	-	10.1	-	ns
Turn-On Rise Time		tr	-	7.3	-	
Turn-Off Delay Time		td(off)	-	31.3	-	
Turn-Off Fall Time		tf	-	28.2	-	

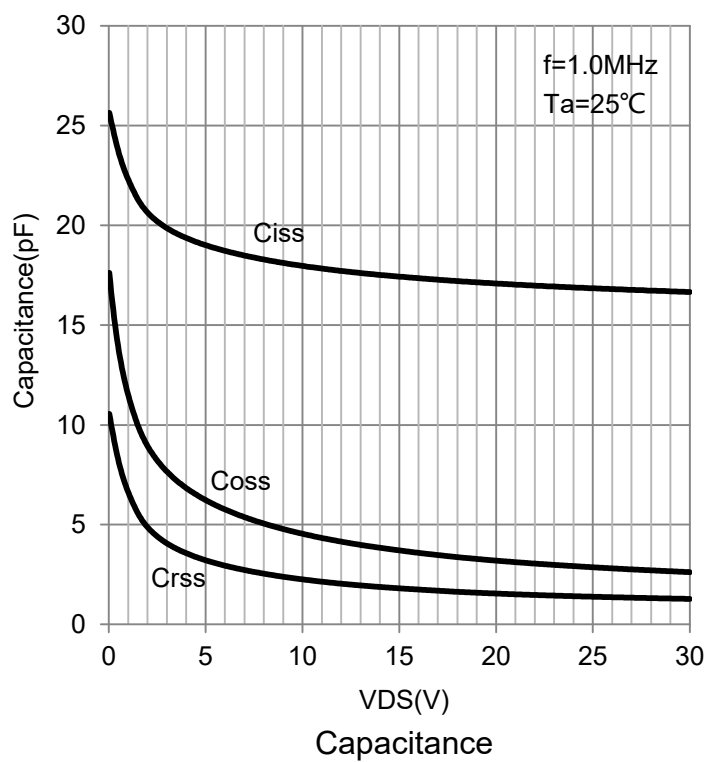
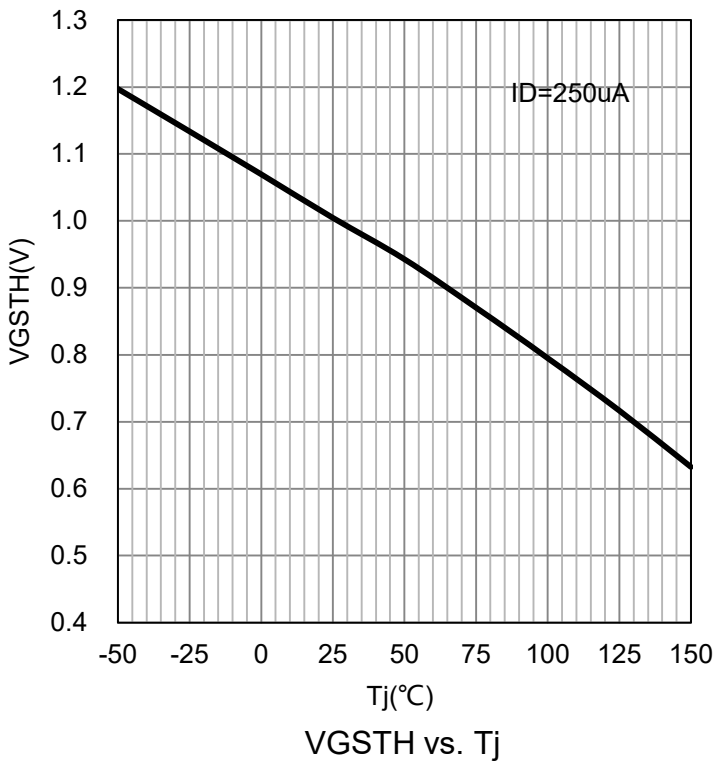
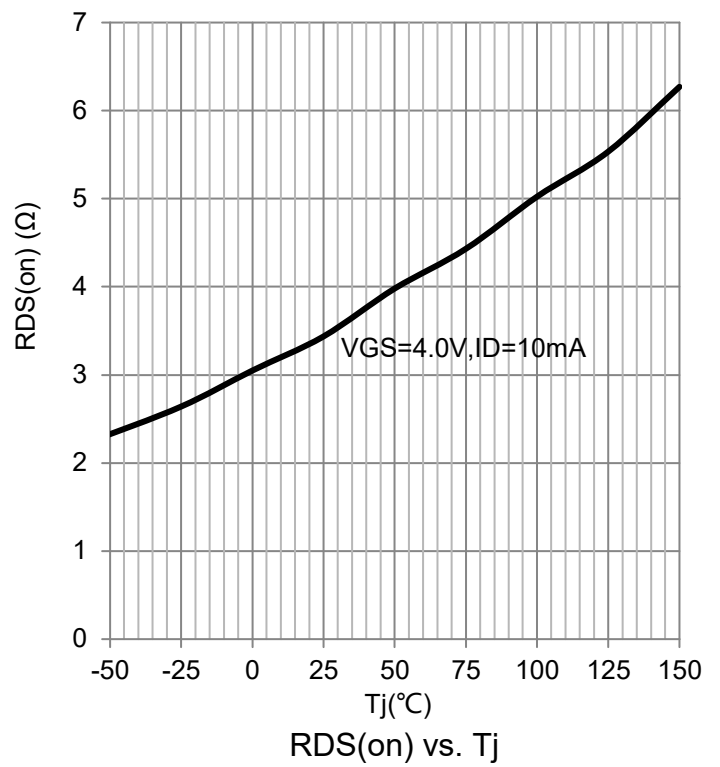
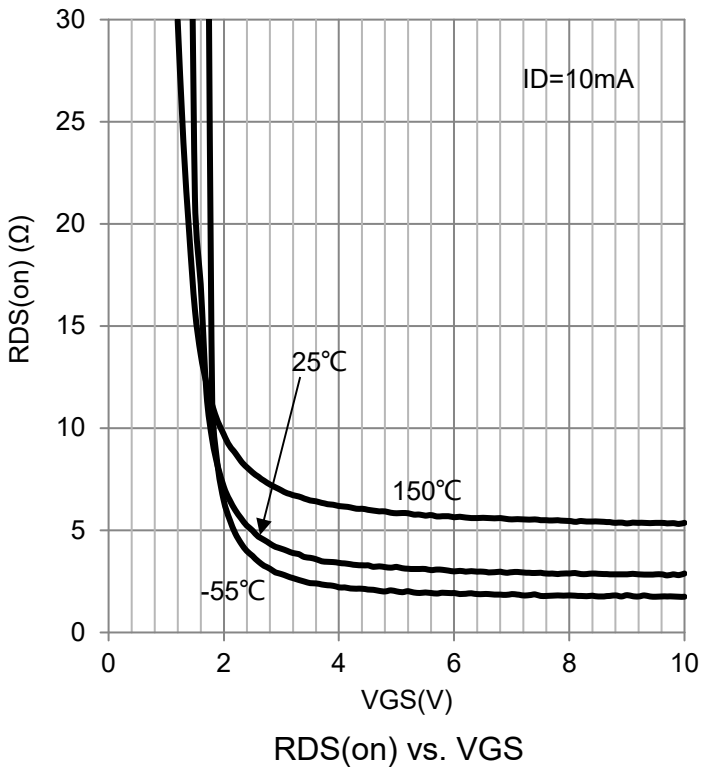
3.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.



7. ELECTRICAL CHARACTERISTICS CURVES



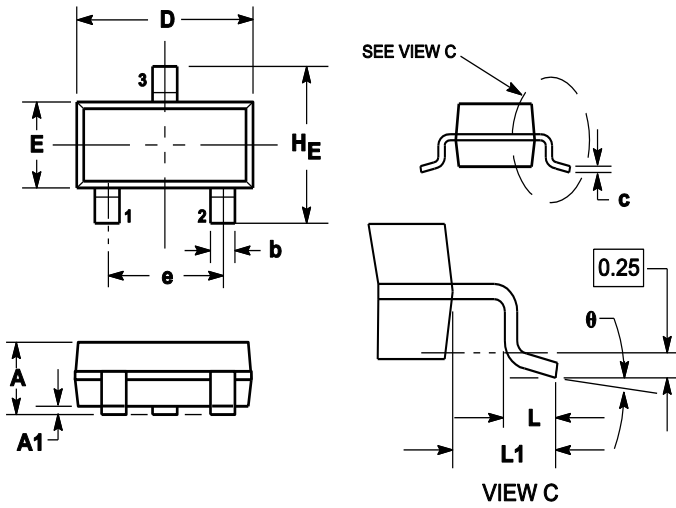
7. ELECTRICAL CHARACTERISTICS CURVES (Con.)



8. OUTLINE AND DIMENSIONS

Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9. SOLDERING FOOTPRINT

